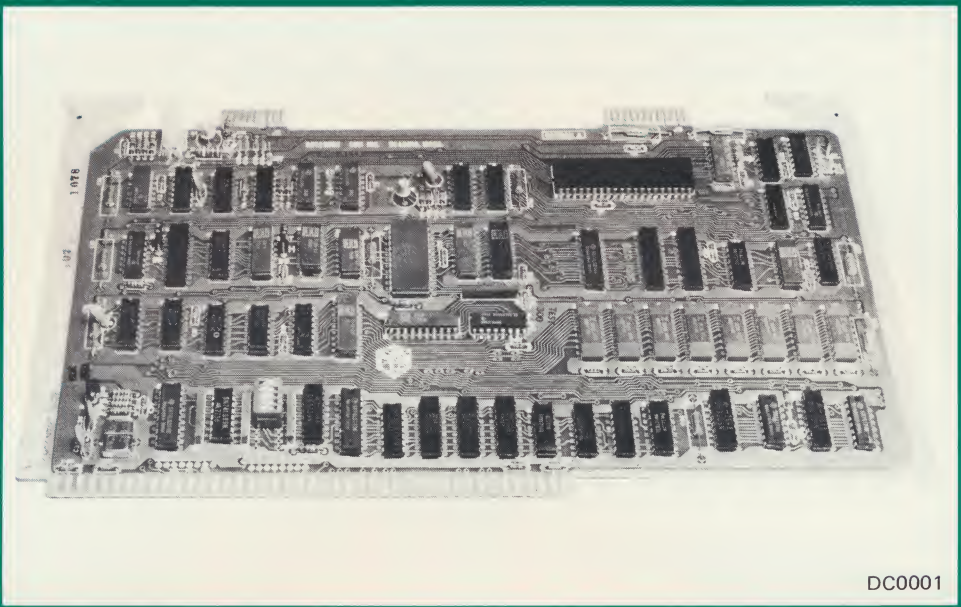
DATACUBE

VideoRam

MODELS VR-107A, VR-109A



DC0001

Video Ram—a versatile series of video display modules for the Intel MULTIBUS™. Generate memory-mapped raster-scan display output for Intel SBC/NSC BLC single-board computers. Provide full program selection among four screen formats, to display as many as 1920 characters from a 128-character font in any combination of normal, reverse, half-intensity blink and underline modes. Mixed graphics, a flashing addressable cursor and an interrupt-driven keyboard port allow complete system applications.

- INTEL MULTIBUS™ & NSC Compatible
- Memory-mapped Characters and Graphics
- Choice of Character Font—
  - -7x7 (VR-107A)
  - -7x9 (VR-109A)
- Programmable Display Format
- Dual Video Outputs
  - -direct (X-Y) drive
  - -composite video
- Mixed Character/Graphics Display—
  as many as 1920 display positions
- Non-Flashing Display at
  DMA Access Rates
- Prom Character Generator—
  128 Characters
- Directly-addressed Flashing Cursor
- Overlaid Character/Attribute Memory for any combination of:
  - -Regular or reverse video
  - -Underline
  - -Half-intensity
  - -Blink
- Memory-Mapped Control and Keyboard Ports
- 20-Bit Address Decode on any
  2K Boundary
- Full Screen Attribute Enable and Blanking

Because every character position is a separate location in main memory, your computer program can selectively write (and read) any of the 1920 positions in the display. A separate, overlaid memory provides the same access for four display attributes for each position. For graphics, the two memories are used together to define the display — a maximum of 120 or 144 pixels high by 160 wide.

These powerful capabilities allow you to easily program special displays — split-screen, text/command, text/directory and scrolling. You can mix characters with graphics for versatile display of graphs or shapes, with supporting text and tables. Under program control, even equipment functions and motion can be vividly shown.

If you require a custom character display font, simply change the on-board plug-in ROM.

Three unique memory locations allow direct program control of all module functions, including screen format, blanking, and display attribute latching and enabling. A fourth location serves as data input port for an external keyboard.

Add your composite video or X-Y drive video monitor and a keyboard for a complete video terminal system.

DATACUBE INC. ● 670 MAIN STREET ● READING, MA 01867 ● 617/944-4600

BASIC FEATURES (all models)

COMPATIBILITY: Intel MULTIBUS™ (SBC-80 computer series);
National Semiconductor BLC-80 series
CHARACTERS/LINE: 80 or 40, program-selectable
CHARACTER LINES: 24 or 12, program-selectable
CHARACTER vs GRAPHIC: program-selectable for each of 1920 screen positions
CURSOR (addressable): program-selectable for any one screen position
BLINK RATE: 1, 2, 4 or 8 Hz, strap selected
DISPLAY ATTRIBUTES — CHARACTERS
REVERSE VIDEO (B-O-W)
HALF-INTENSITY
UNDERLINE
BLINK
} Program-selectable for each of 1920 max. screen positions (characters only) and enabled individually for entire screen.
BLINK RATE: 1, 2, 4, or 8 Hz, strap selected
VERTICAL FREQUENCY: 60 Hz (50 Hz optional)
PERIOD: 16.7 msec.
COMPOSITE VIDEO LEVELS (75-ohm termination)

SYNC	0.0 Volts
BLANK	0.4
BLACK	0.5
WHITE	1.5

DIRECT DRIVE (X-Y) COMPATIBILITY
Most popular video data displays, including:
BALL BOTHERS, Models TV-5, TV-9, TV-12, TV-120
MOTOROLA, Models M-1000. M-2000, M-3000, M-4000

OPTIONS (all models)

ALTERNATE CHARACTER FONTS (special order)
VERTICAL FREQUENCY: 50 Hz (special order)

CABLE ASSEMBLIES (all 3ft. — 1M)	PART NO.
KEYBOARD PORT RIBBON CABLE, CONNECTOR	C-10001
DIRECT DRIVE RIBBON CABLE, CONNECTOR (for Ball Bros. or Motorola monitor)	C-10002
COMPOSITE VIDEO CABLE, CONNECTOR	C-10003

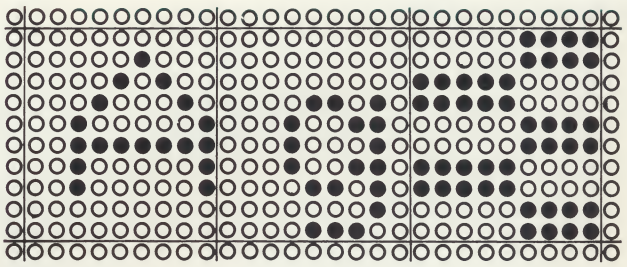
KEYBOARD ASSEMBLY (Models SMK 53, 62, 73 and 86)
ASCII-encoded, 53 to 86-key, w/cable, connectors
Solid/state capacitive-key, N-Key rollover

MODEL VARIATIONS

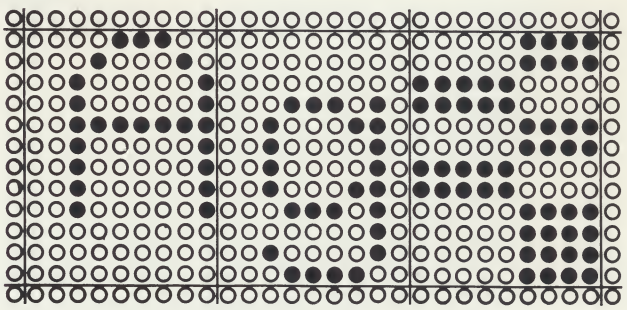
MODEL VR-	107A	109A
ADDRESSING FORMAT	BINARY	BINARY
MEMORY SPACE	2048	2048
CHARACTER MATRIX (HxV)	7x7	7x9
BLOCK	9x10	9x12
GRAPHIC MATRIX	2x5	2x6
HORIZONTAL, tot	160	160
VERTICAL, tot	120	144
TIMING-HORIZONTAL		
HORIZONTAL FREQ. (KHz)	15.72	18.6
PERIOD (usec)	63.61	53.76
DLY BEFORE SYNC	2.54	2.1
SYNC	5.08	4.2
DLY AFTER SYNC	5.08	5.3
BLANKING	12.72	11.5
DRIVE (BALL BROS.)	27.5	27.5
MOTOROLA	5.08	4.2
TIMING-VERTICAL		
DELAY BEFORE SYNC (usec)	191	0
SYNC (usec)	191	215
DELAY AFTER SYNC (usec)	954	968
BLANKING (msec)	1.4	1.18
DRIVE (BALL BROS.) (msec)	1.4	1.18
(MOTOROLA) (usec)	191	215

CHARACTER FONT

VR-107A—7x7



VR-109A—7x9



DATA AND CONTROL PORTS

WRITE FUNCTION			BIT	READ FUNCTION
ATTRIBUTE PORT	(base address + 7FC HEX)			
Video Latch	0=NORM	1=REV	0	Attribute Latch — contents automatically transferred to attribute memory for each character written to data memory when attribute mode is auto (Format Port Bit 3=1)
Half-Inten. Latch	0=CLR	1=SET	1	
Underline Latch	0=CLR	1=SET	2	
Blink Latch	0=CLR	1=SET	3	
Video Enab.	0=NORM	1=REV	4	Enable entire screen
Half-Inten. Enab.	0=DIS	1=ENAB	5	
Underline Enab.	0=DIS	1=ENAB	6	
Blink Enab.	0=DIS	1=ENAB	7 (MSB)	
KEYBOARD PORT	(base address + 7FD HEX)			
			0	Data bit 0
			1	1
			2	2
	WRITE IGNORED		3	3
			4	4
			5	5
			6	6
			7 (MSB)	7 (MSB)
FORMAT PORT	(base address + 7FE HEX)			
Kybd IRQ Stat (Internal Use Only)	0=INACT.	1=IRQ	0	Not available
			1	Kybd data 1=RDY 0=NOT RDY
Kybd IRQ	0=DIS	1=ENAB	2	See VideoRam Applications Bulletin
Attrib.WR Mode	0=MAN	1=AUTO	3	
Read mem	0=DATA	1=ATTRIB	4	
V Format	0=12	1=24	5	
H Format	0=40	1=80	6	
Disp. Blank	0=DISP	1=BLANK	7 (MSB)	

CONTROL PORT (base address + 7FF HEX)

Write 86 HEX to this port to initialize VideoRam

For other write functions, see VideoRam Applications Bulletin

SPECIFICATIONS (all models)

MEMORY ADDRESSING

Overlaid Display and Attribute memory, 2048 locations each
20-bit address decode—select any 2K memory boundary
1920 Display/Attribute bytes
112 read/write memory locations, unassigned
16 (4 groups of 4) Data and Control registers

INTERRUPTS

Single-level keyboard interrupt, strappable to any one of eight interrupt request lines — program-enabled.

INTERFACES

BUS: all signals TTL-compatible
PARALLEL (keyboard) I/O: All signals TTL-compatible

CONNECTORS

INTERFACE	NO. OF PINS	CENTERS (IN.)	MATING CONNECTORS
Bus	86	0.156	CDC VPB01E43A00A1
Keyboard	26	0.1	3M 3462-0001 or TI H312113
VIDEO			
Direct Drive	20	0.1	3M 3461-0001
Composite	2	0.156	MOLEX 09-50-3021

BUS DESCRIPTION

See Intel Applications Note AP-28.

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.5 cm.)
Height: 6.75 in. ref. (17.1 cm.)
Depth: 0.50 in. max. (13 mm.)
Weight: 18 oz. (500 g.)

ELECTRICAL CHARACTERISTICS

DC Power: (all voltages ±5% tolerance)
5 volts, 3 amperes
12 volts, 0.1 ampere
-12 volts, 0.1 ampere

ENVIRONMENTAL

Temperature:
Operating: 0 to 55° C (32 to 131° F)
Storage: -40 to 100° C (-40 to 212° F)

DISPLAY FORMATS (all models)

CHARACTER LINES	POSITIONS PER LINE	
	80	40
24	1920 (no line space)	960 (no line space)
12	960 (one line space)	480— DOUBLE SIZE (no line space)

PROGRAMMING NOTES

INITIALIZE ROUTINE

1. Write 86 HEX to Control Port to set up VideoRam system;

2. Write 01 HEX to Format Port to:
   - blank display;
   - disable keyboard interrupt;

3. Write 00 HEX data to Attribute Port to:
   - disable all attributes;
   - clear attribute latch;

4. Set computer memory pointer to base address chosen for VideoRam display memory;

5. Write 1920 (decimal) sequential bytes of 20 HEX data (space code) to display memory to clear display;

6. Write video display and video latch display formats to Attribute Port (8 bits);

7. Write control byte desired Format Port, to:
   - select character attribute source (latch or external write);
   - select H and V display formats;
   - select future display memory reads to be from either attribute or data memory;
   - enable keyboard interrupt (if desired);
   - unblank display;

8. Write cursor command (90 HEX) to desired cursor address (anywhere in display memory);

GRAPHICS DISPLAY ROUTINE

1. Same as character display routine;

2. Fetch and write elements for part of graphics block (00NN NNNN BINARY, where NN NNNN are elements G6 to G1);

3. Fetch and write elements for rest of graphics block (11NN NNNN BINARY, where NN NNNN are elements G12 to G7);

4. Go to step 1 for next graphic element.

CHARACTER DISPLAY ROUTINE

1. Set computer memory pointer to address (position) desired in display memory;

2a. Set Format Port Bit 3 to 1 if standard (latched) attributes are desired; otherwise:

2b. Fetch and write attributes for character (1000 NNNN BINARY, where NNNN are attribute bits);

3. Fetch and write character data byte (0NNN NNNN BINARY);

4. Update cursor by writing 90 HEX to desired cursor address (anywhere in display memory);

5. Go to step 1 for next character.

DISPLAY MEMORY READ

1. Set computer memory pointer to address of character or graphics block desired for read;

2. Set Format Port Bit 4 to 1 to enable attribute memory read;

3. Read and store character attributes or graphic elements G12 to G7 (1SNN NNNN BINARY, where S=1 for graphics and S=0 for attributes and NN NNNN are graphics or attribute data);

4. Set Format Port Bit 4 to 0 to enable data memory read;

5. Read and store character data or graphic elements G6 to G1 (0NNN NNNN BINARY, where NNN NNNN are graphics or character data);

6. Go to step 1 for next character.

MEMORY ADDRESSING

BINARY ADDRESSING

Models VR-107A and VR-109A use efficient binary addressing, where display positions are accessed sequentially, in normal reading order. These models may be strapped for an address origin on any 2K memory boundary, and use a contiguous 2048-address memory segment, all active.

Locations from ORIGIN + 780 HEX to ORIGIN + 7EF HEX are available as unassigned read-write memory, in the same manner as data and attribute memory.

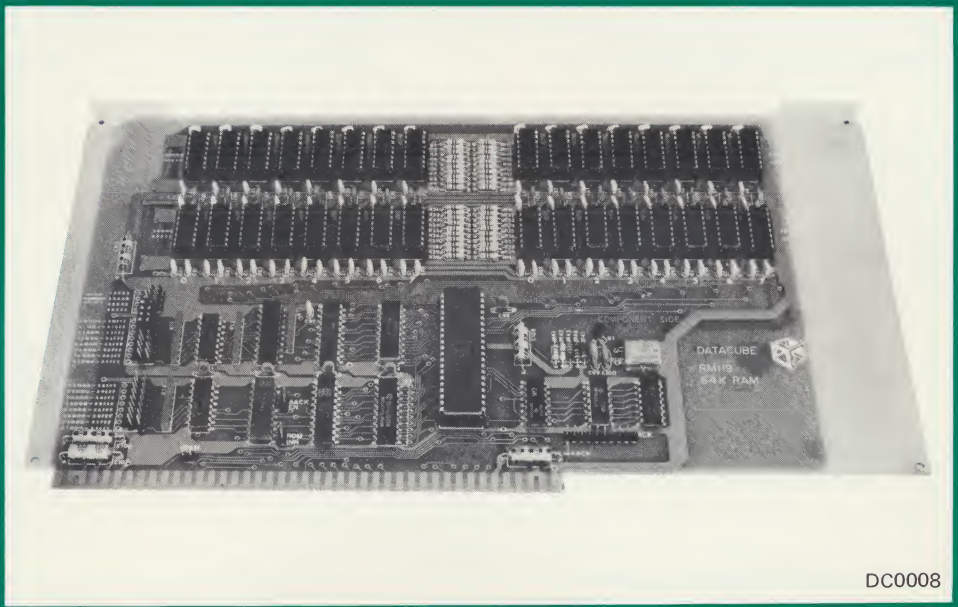
Data and Control ports appear at the end of the memory block, as follows:

Attribute Port: ORIGIN + 7FC HEX
Keyboard Port: ORIGIN + 7FD HEX
Format Port: ORIGIN + 7FE HEX
Control Port: ORIGIN + 7FF HEX

When 40-column format is selected, the last (righthand) 40 memory positions for each line are unused. When 12-line format is selected, the last (bottom) 12 lines of memory are also unused.

DATACUBE

MODEL RM-119
64K DYNAMIC READ/WRITE MEMORY



DC0008

High-density dynamic read/write memory for the Intel MULTIBUS. Provides as many as 64 kilobytes of memory for the Intel SBC / NSC BLC single-board computers. Industry-standard 16K (4116) memory is used.

Data are selected by a 20-bit address and appear on the bus as 8-bit bytes.

- Intel MULTIBUS™ and NSC Compatible
- Dense Dynamic Read/Write Memory — 4116 Type
- 20-Bit Address Bus — also Compatible with 16 Bits
- Five Versions: 16, 32, 48 or 64 Kilobytes or Unpopulated (All Versions Fully Socketed)
- Independent Memory Disable for 16 4K Blocks
- On-Board Memory Refresh — Minimal Overhead
- Advanced LSI Memory Control for Cost Effectiveness and Low Energy Demands
- High-Reliability Side Grip Sockets — Deep Pin Ramps for Easy Insertion

High-density dynamic read/write memory is ready for your system applications. Model RM-119 makes efficient use of your module slots with as many as 64K on one module.

Use the RM-119 in current 16-bit address systems and instantly expand to 20 bits when you need it.

RM-119 employs an advanced LSI memory and refresh control device, to reduce parts count for reliability and economy.

You can use address space flexibility because memory can be selectively disabled for each of sixteen 4K blocks. Disabled memory is totally transparent to the bus.

DATACUBE INC. ● 670 MAIN STREET ● READING, MA 01867 ● 617/944-4600

SPECIFICATIONS

MEMORY ADDRESSING

20-bit address selection — compatible with 16 or 20-bit address bus. Addressed as one bank of 64 kilobytes, selectable for an origin on any 64K address boundary. Each 4K block individually jumper-disabled.

DEVICE COMPATIBILITY

Read/write memory: provided as industry-standard 4116-type dynamic memory devices — max. 32 per module.

DATA BUS TIMING

Max. 350 nsec access time for read or write.

Max. 550 nsec memory cycle time.

On-board refresh requires 0.5 microseconds from bus each 12 microseconds, approx. Refresh degrades read/write memory response approx. four percent.

DATA BUS SIZE

Eight-bit data, MULTIBUS-compatible.

BUS DESCRIPTION

All signals TTL-Compatible.
See Intel Applications Note AP-28a.

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.5 cm)
Height: 6.75 in. ref. (17.1 cm)
Depth: 0.50 in. max. (13 mm)
Weight: 16 oz. (455 g.), fully populated

ELECTRICAL CHARACTERISTICS

DC Power (all voltages ±5% tolerance):
+ 5 volts, 1 ampere max., fully populated
− 5 volts, 0.01 ampere
+ 12 volts, 0.5 ampere

CONNECTORS

INTERFACE	NO. OF PINS	CENTERS (in.)	MATING CONNECTORS
Bus	86	0.156	CDC VPB01E43A00A1

VERSIONS

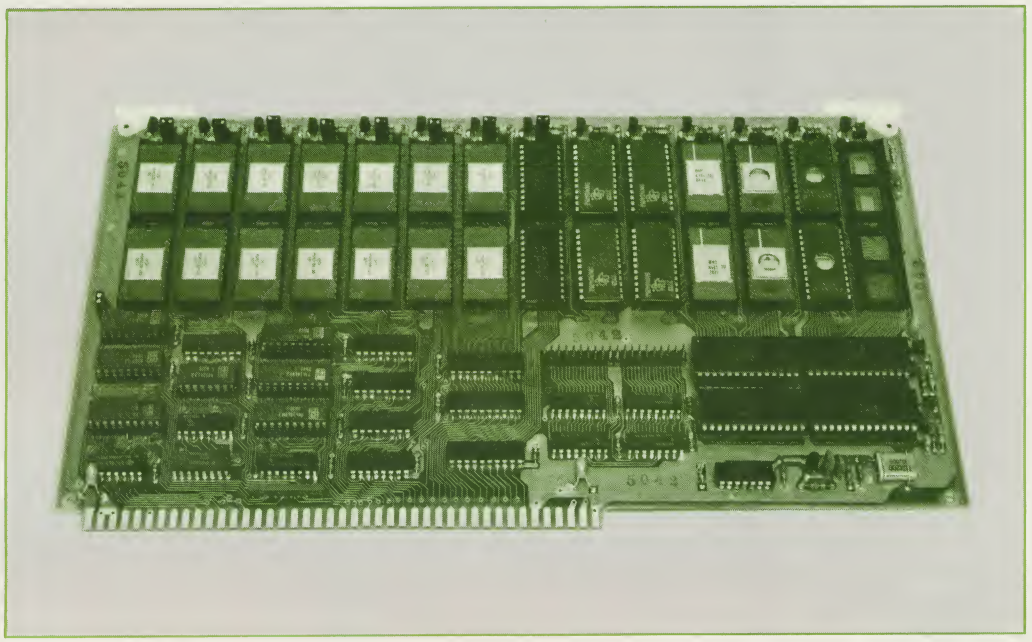
All versions fully socketed for 64KB read/write memory.

RM-119-UP	memory unpopulated
RM-119-016	16 kilotypes dynamic read/write memory
RM-119-032	32 kilobytes
RM-119-048	48 kilobytes
RM-119-064	64 kilobytes

DATACUBE INC. ● 670 MAIN STREET ● READING, MA 01867

Datacube INC.

MODEL CM-126A
UNIVERSAL MEMORY



A complete memory resource on one MULTIBUS™ module. Provides system access to as many as 32 user-installed RAM, PROM and ROM memory devices in any combination by pairs, anywhere within a 20-bit address space. As much as 500 kilobytes of memory within a 1 megabyte range, for 8 or 16-bit data.

- **Intel MULTIBUS™ and NSC Compatible (Proposed IEEE 796 Bus Standard)**
- **High Density Memory—to .5 Megabyte EPROM**
- **Each Device Addressed as n Unique 1K Byte Blocks—Overlay Any Block on Any 1K Boundary**
- **Accepts over 15 5-Volt Byte-wide Memory Types—4K to 128K Bits each, MOS or Bipolar**
- **Full 20-Bit Address Bus—1 Megabyte Range**
- **All Data Access Types:**
  - **byte-sequential (8080)**
  - **word-parallel (8086)**
  - **interleaved bytes (8088)**
- **Accepts 32 Memory Devices—each pair:**
  - **address on any 1K boundary**
  - **selectable access time**
  - **power strobe enable**
- **Accepts Mixed ROM/PROM/EPROM and RAM**
- **Device Power Strobe for Low Current**
- **Quality 28-pin DIP sockets provided—accept 24 or 28-pin devices**
- **Crystal-Controlled Device Access Time—50 ns Access Resolution, 80-800 ns Range**
- **Designed for Computerized High-Speed Testing**

Nearly every system memory requirement can now be met with a single module. CM-126 puts any mix of byte-wide memory devices on the MULTIBUS, for systems with 8 or 16-bit data access (or mixed 8/16 bit).

You can use RAM, ROM, PROM, EPROM and EEPROM devices in any combination. And, each 1K segment of any device pair can be mapped uniquely to any 1K address within the megabyte system range. Read/write and read-only memory can overlay external memory freely, for example, to create "shadow" ROM areas for startup, or to "patch" ROM areas using RAM.

Thirty-two DIP sockets on CM-126 accept fifteen generic memory types, MOS or bipolar — from 4K to the latest 128K products — and even read the new electrically-erasable ones. You can select access time and optional automatic power strobe for each pair of devices, to optimize performance.

DATACUBE INC. ● 670 MAIN STREET ● READING, MA 01867 ● 617/944-4600 TWX 710/393-0144

SPECIFICATIONS

DEVICE COMPATIBILITY

Accepts most industry-standard 5-volt, 8-bit data width read/write and read-only memory devices. Devices are 24 or 28-pin package, 0.6 in. (15.25 mm.) on centers. Install 24-pin types so that pin 1 of package is in pin 3 of 28-pin socket. Install devices of any kind in any socket, but only in pairs of the same type and access speed.

Memory device type and memory access time are selected for each pair of devices by an on-board fusible-link PROM. See Selection PROM coding information below.

CM-126A accepts programmable devices for read only.

See table of compatible devices.

MEMORY ADDRESSING

Address bus 20 bits—for one megabyte address range. Sixteen-bit address compatibility automatically provided by internal pullup resistors which default 4 MSB to logic zero.

Maximum 32 user-installed memory devices, addressed as sixteen pairs. Both devices of a pair must be the same type. Each 1K segment of any pair can be mapped with its base at any 1K boundary anywhere within the megabyte address range of the bus. Thus, any 1K segment can overlay any other 1K segment of any device installed on CM-126.

Overlay control is provided as part of the address translation; see below. Each onboard RAM or ROM segment can provide INH1 or INH2 to the bus when selected, to overlay external memory. Conversely, external memory can overlay any on-board memory segment which does not generate an inhibit.

Address Translation

Mapping of the 20-bit MULTIBUS address into 1K segments of a pair of devices is made by on-board fusible-link PROMs. The output of the PROMs enables a particular 1K segment of the user devices, and selects other options. Translation PROMs are provided unprogrammed (disabling all memory devices), and are user-programmed as desired. See Translation PROM coding example.

DATA WORD SIZE

Full 16-bit data bus, compatible with 8, 16 or mixed 8/16 MULTIBUS transactions. Byte-sequential (for 8080), word-parallel (8086) and interleaved bytes (8088/8086) access controlled by ADR0 and BHEN, using an on-board swap-byte buffer.

Eight-bit-only response selected for each pair of devices by address translation PROMs. See Translation PROM coding example.

BUS DESCRIPTION

All signals TTL-compatible.

See Intel MULTIBUS Specification 9800683, Intel Application Note AP-28A and IEEE Proposed 796 Bus Standard.

IEEE 796 Bus Compliance A20 and D16.

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.5 cm.)
Height: 6.75 in. ref. (17.1 cm.)
Depth: 0.50 in. max. (13 mm.)
less user-provided devices
Weight: 11 oz. (320 g.)

ELECTRICAL CHARACTERISTICS

DC Power: +5 volts, ±5% tolerance; 1.8 ampere

Current shown is for unloaded board; add current of installed memory devices for total.

ENVIRONMENTAL

Temperature:
Operating: 0 to 55° C (32 to 131° F)
Storage: -40 to 100° C (-40 to 212° F)
Humidity: 10 to 90% RH, non-condensing

COMPATIBLE DEVICES (partial listing)

Device type codes shown in parentheses.
Programmable devices must be programmed external to CM-126.

DEVICE TYPES	BYTES STORAGE, each device						
	256	512	1K	2K	4K	8K	16K
Read/Write			4000(5H) 4118(5H)	4016(7H) 6116(7H) 21R1(7H)			
EPROM			2508(4H) 2758(4H)	2516(6H) 2716(6H)	2532(CH) 2732(8H)	2564(EH) 2764(9H)	2528(FH)
Fusible-Link PROM	6336*(0H)	6341(1H)	74S478(2H) 87S228(2H) 3628(2H) 5618(2H) 6381(2H) 6384(2H) 7681(2H) 93451(2H)	63S1681(3H) 82S191(3H) 2616(6H)			
Masked ROM Most masked ROMs which are replacements for EPROMS shown above are compatible.			6281(2H)	2316E(6H) 6276(6H) 34000(6H)		2364(9H) 3565(9H) 37000(AH)	
EEPROM				28E1(BH)			

*NOTE: 256x8 devices require 2Kx4 translation PROMs installed at U33 and U34 in lieu of 1Kx4 PROMs supplied.

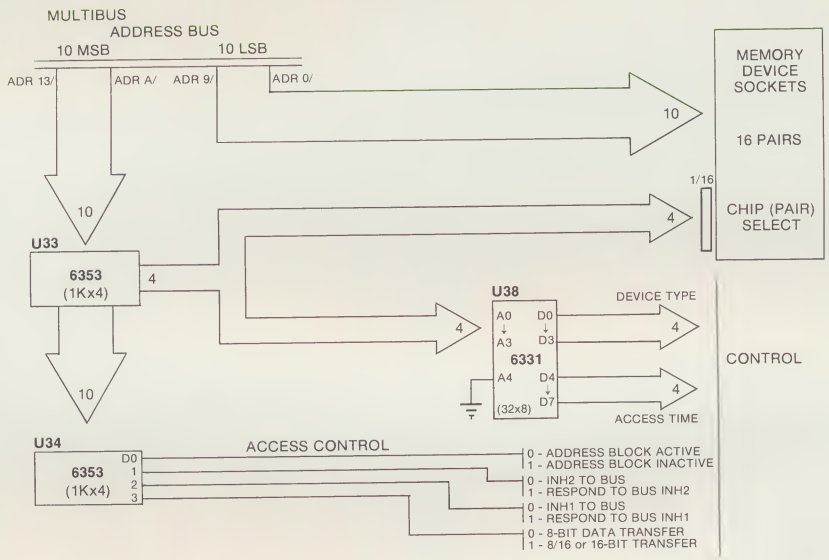
ADDRESS SYSTEM

CM-126 divides the 20-bit MULTIBUS address range into 1024 possible 1K segments; each memory device or device pair contains one or more segments. Control PROMs translate each memory segment access into a unique memory device socket pair with its associated device type and access time, and also selects access control functions. Thus, any 1K segment of any memory device pair can be mapped on a 1K boundary anywhere within the full megabyte address range, and any 1K segment can overlay any other segment. The segments actually usable are limited by memory density; a CM-126 fully populated with 16-kilobyte EPROMs contains 512 1K memory segments.

CM-126 controls on-board memory access using three PROMs — U33, U34 and U38. As shown in the drawing below, the MULTIBUS address 10 LSB directly select one of 1K addresses at the device sockets. The 10 MSB address bits are presented to both U33 and U34, selecting one of the 1024 addresses in each PROM, representing all possible memory device segments.

Each location in U33 contains a 4-bit data value used to select one of the sixteen device socket pairs. The same 4-bit value is the address to U38, which provides two 4-bit data values (also unique to the selected socket pair). U38's 4 MSB select the device pair access time, and the 4 LSB characterize the device type. (Thus, both type and access time are the same for both devices of the pair.)

U34 provides a unique 4-bit activity control pattern for each of its 1024 locations. This pattern controls whether the selected memory segment is active on the bus, and if so, whether it provides byte-sequential or word-sequential data transfers, and whether CM-126 must generate or respond to the MULTIBUS overlay controls INH1 and INH2.



PROGRAMMING CONTROL PROMS

1. Determine the 20-bit base address for each 1K segment of each memory device (if byte-sequential) or of each device pair (if alternate bytes or word-sequential access). Allowable base addresses are nn000, nn400, nn800 and nnC00 HEX, where nn is 00 to FF HEX.

2. Determine the control PROM addresses corresponding to each of the memory segments found above:
   —write the 10 most significant bits of a segment as binary;
   —invert the bits (1's complement);
   —write the resulting number as 3 HEX digits.
   Example—20-bit MULTIBUS base address 4F800 HEX:
   10 MSB = 0100111110
   INVERT = 1011000001
   HEX = 2 C 1
   This is the address of PROMs U33 and U34 for this segment.

3. Generate the contents of PROMs U33 and U34. Assign sockets for each device (arbitrary, except that socket pairs must contain only devices of the same type and access time). For each PROM address found in step 2:
   —program PROM U33 with the 4-bit memory device socket pair 0 to F HEX containing the 1K memory segment;
   —program PROM U34 with the four-bit binary activity code (as shown in the drawing) for the same 1K segment.

4. Generate the contents of PROM U38. Determine the type and access speed of each memory device to be used. (U38 contains 32 8-bit values from 0 to 1F HEX; only the 16 locations from 0 to F HEX are used. These locations correspond to the 16 memory device socket pairs.)
   —For each location, program the 4 MSB with the device access time and the 4 LSB with the device type from the table below.

U38 PROM DATA TABLE

HEX VAL	4 MSB ACCESS TIME	4 LSB DEVICE
0	80 typ.	6336
1	130 max.	6341
2	180 max.	6281/6381
3	230 max.	63S1681
4	280 max.	2758
5	330 max.	4118
6	380 max.	2316/2616E/2716
7	430 max.	6116
8	480 max.	2732
9	530 max.	2364/2764
A	580 max.	37000
B	630 max.	28E1
C	680 max.	2532
D	730 max.	-spare-
E	780 max.	2564
F	830 max.	2528

(Addresses 10 to 1F HEX are unused.)

NOTE: If CM-126 asserts INH1 or INH2 inhibit signals, access time is automatically extended to 1.6 microseconds for that cycle.

NOTE: PROMs supplied are all 1's before programming, disabling all memory segments. Some PROMs available are all 0's before programming, and must be programmed in all locations to ensure inactive segments are disabled.

DATACUBE will custom-program CM-126 control PROMs to match your memory configuration for a one-time setup charge. Contact the Applications Department.

APPLICATION EXAMPLE

CM-126 is adaptable to a wide variety of MULTIBUS system designs. Because it accepts most byte-wide memory devices and permits extremely flexible addressing, this one module can accompany your product from prototype through production phases.

This example describes a computer design which uses one memory mix and size for development and another for production. In both cases, CM-126 efficiently replaces two or three ordinary MULTIBUS memory modules.

Development

Here, the design requires a small ROM monitor program to provide program loading, running and simple debugging utilities. An experimental high-speed math package contained in bipolar PROM is being tested. The user program is being developed in RAM, which is also used for data scratch storage. (On startup, the ROM monitor overlays or "shadows," RAM.) CM-126 is fully populated, with a memory mixed both in type and speed.

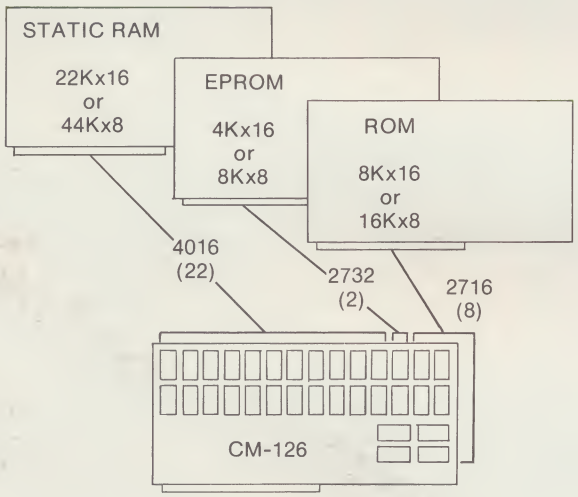
Production

With the design complete, the RAM used for experimental code is replaced by EPROM containing the user program. The math package remains in bipolar PROM because of its superior access time. The needs for scratch RAM and startup monitor remain.

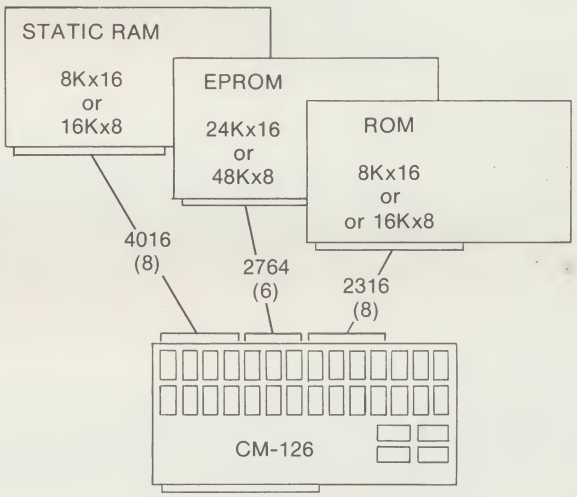
Ten memory device sockets remain open for later additions of memory to accommodate field upgrades.

CM-126 is reconfigured for the new memory requirements by programming the inexpensive selection and translation PROMs. One effective method of customizing the product is to distribute selection PROMs coded to activate selected options embedded in the program. You can activate diagnostic program segments in the same manner — without removing or unstrapping installed memory devices. The fine address granularity allows effective use of memory space.

DEVELOPMENT



PRODUCTION

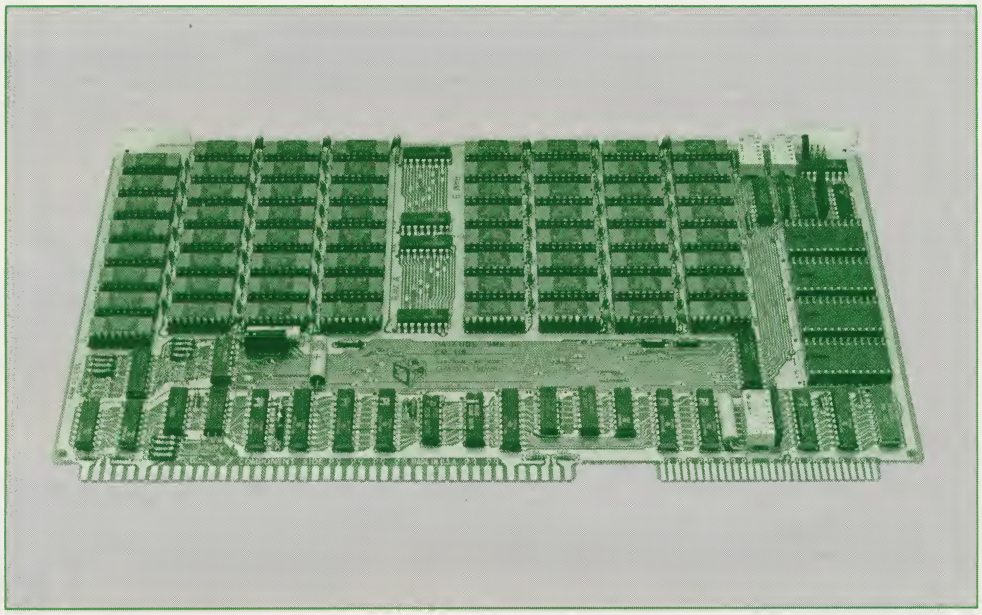


DATACUBE INC. ● 670 MAIN STREET ● READING, MA 01867

PRINTED IN U.S.A./CM-126A, R0 8104-10M (DaySys)

DATACUBE

MODEL CM-118
32K STATIC READ/WRITE MEMORY



High-density static read-write memory for the Intel MULTIBUS™. Provides 32 kilobytes of memory for the Intel SBC / NSC BLC single-board computers. Reliable 4K (2114-type) memory is used, in your choice of speeds. Also accepts 8K of industry-standard PROM or ROM.

Data are selected by a 20-bit address and appear on the bus as 8-bit bytes.

- **Intel MULTIBUS™ and NSC Compatible**
- **Dense Static Read/Write Memory—2114 Type**
- **16-Bit/20-Bit Address Bus—User Option**
- **Two 16K Memory Banks with Independent Base Addresses**
- **8K ROM/PROM Sockets with Independent Base Address**
- **Two Memory Device Speed Options—or Unpopulated Module**
- **Selectable Access Time Delay for Slower Memory Devices**
- **High-Reliability Side-Grip Sockets—Deep Pin Ramps for Easy Insertion**
- **Expansion Memory for RM-117 (high-speed model only)**

You can now select reliable static read-write memory for your system applications. Model CM-118 gives you 32K on one module—and a bonus of 8K ROM/EPROM sockets.

Use the CM-118 in current 16-bit address systems and instantly expand to 20 bits when you need it.

A high-speed version of CM-118 provides quick expansion for the RM-117 dual-port memory system.

You can use address space flexibly because memory is addressed as two 16K banks with separate switch-selected origins. ROM has its own selectable origin as well.

Choose high-speed memory for quick data access or low speed for economy. Or—use your own memory devices in an unpopulated CM-118. Select from a wide variety of access times to accommodate any memory component.

DATACUBE SMK INC. ● 670 MAIN STREET ● READING, MA 01867 ● 617/944-4600 ● TWX-710-393-0144

SPECIFICATIONS

MEMORY ADDRESSING

Read/write memory: two banks of 16 kilobytes each; each bank independently selectable for an origin on any 16K address boundary.

Read-only memory: one contiguous bank of 8 kilobytes; independently selectable for an origin on any 8K address boundary. Each socket individually enabled; disabled device will not generate acknowledgement to bus access.

20-bit address selection—compatible with 16 or 20-bit address bus. Address origin selected by DIP slide switches.

DEVICE COMPATIBILITY

Read/write memory: accepts industry-standard 2114-type static memory devices—max. 64 per module.

Read-only memory: accepts one to four industry-standard 24-pin ROM, PROM or EPROM devices (eg. 2716 EPROM, 2616 PROM, 3216 ROM).

Independent transfer acknowledge delay for read/write and read-only memory: delay range 0 to 15 bus clock periods.

DATA BUS SIZE

Eight-bit data, MULTIBUS™ compatible.

BUS DESCRIPTION

All signals TTL-compatible.

See Intel Applications Note AP-28A.

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.5 cm.)
Height: 6.75 in. ref. (17.1 cm.)
Depth: 0.50 in. max. (13 mm.)
Weight: 18 oz (515 g.), populated

ELECTRICAL CHARACTERISTICS

DC Power (all voltages ±5% tolerance):
+5 volts, 1 ampere, unpopulated
6.5 ampere max., —fully-populated with 200 ns devices

ENVIRONMENTAL

Temperature:
Operating: 0 to 55°C (32 to 131°F)
Storage: -40 to 100°C (-40 to 212°F)

CONNECTORS

INTERFACE	NO. OF PINS	CENTERS (IN.)	MATING CONNECTORS
Bus	86	0.156	CDC VPB01E43A00A1
Auxiliary	60	0.100	CDC VPB01B30A00A1

VERSIONS

		RM-117 Compatible
CM-118	32K read/write memory, 200 ns.	YES
CM-118-SL	32K read/write memory, 450 ns.	NO
CM-118-SL-16K	16K read/write memory, 450 ns.	NO
CM-118-UP	no memory devices; full socketed for max. 32K devices (64 sockets)	NO

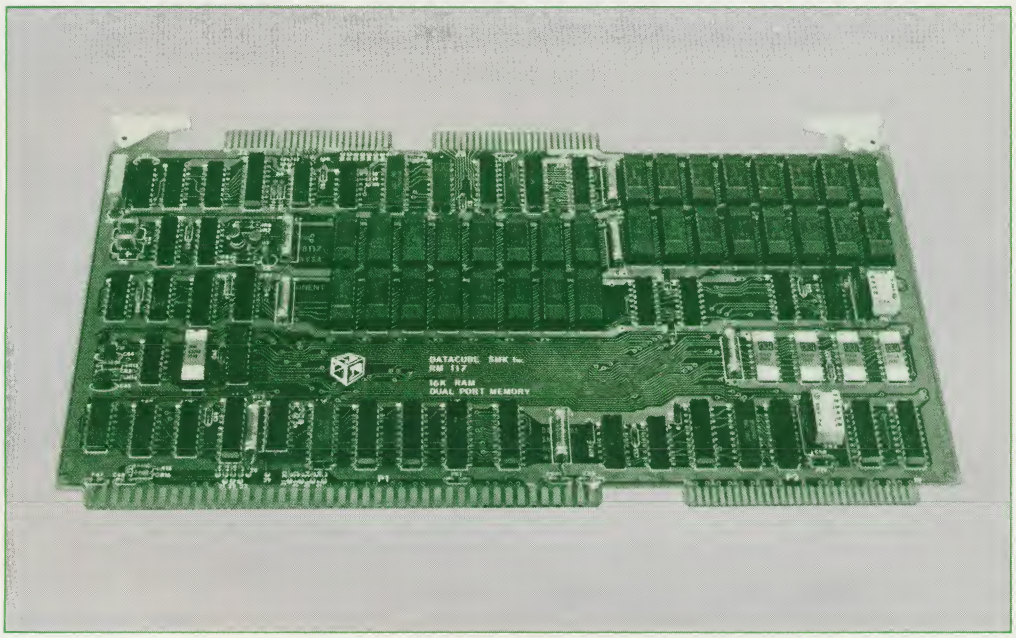
NOTE: All versions provide four 2K ROM/PROM sockets.

Printed in U.S.A. / CM-118, R0 7905-10M (DAY)

DATACUBE INC. ● 670 MAIN STREET ● READING, MA 01867

DATACUBE

DUAL-PORT MEMORY
MODEL RM-117



A complete memory management system for the Intel MULTIBUS™. Allows two independent MULTIBUS ports to share access to a common memory area. Onboard 16K memory can be expanded to one megabyte using external modules.

Designed for dual-processor systems, the PM-117 gives you full read or write access control for each port. Programmable registers provide address translation from 16 to 20 bits, for a full megabyte of virtual memory.

- Dual-Port Memory Management
- Intel MULTIBUS™ & NSC Compatible
- 1 Megabyte Virtual Address Space — 65K Map per Port
- 16K Read-Write On-Board Memory
- 16 or 20-Bit Port Address Bus — Automatic 20-Bit Address Translation for 16-Bit Memory Address
- Dual-Processor Ports — Complete Control & Contention Logic
- Full-Speed Memory Access

EACH PORT

- Address Translation for Eight 8K Memory Banks
- Full Multibus Signal Compatibility;
- Isolated I/O Command System
- Access Control to Exclude Other Port on Read and/or Write
- Bank Enable for Each Memory Bank
- Master Enable for Entire Port
- Read and Write Access Control; Interrupt on Access Violation

---

Each MULTIBUS master port has address translation and control registers for eight 8K memory blocks. Using I/O commands, you can program each bank to be on any 8K boundary in a virtual 1-megabyte (20-bit) memory space.

You can enable or disable any bank and restrict read and/or write access of any bank by the other port. An interrupt occurs whenever a prohibited access is attempted.

Automatic access timeouts prevent a port from locking up the system, and a protect override allows a privileged access for status handshaking.

DATACUBE SMK INC. • 670 MAIN STREET • READING, MA 01867 • 617/944-4600 • TWX-710-393-0144

SPECIFICATIONS

I/O SYSTEM

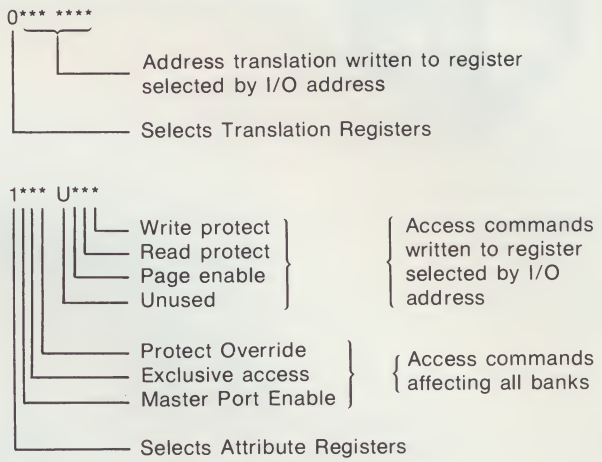
I/O operations are write-only, for module command.
Separate I/O system for each of two master ports.
Strap I/O base address to any boundary in increments of 8, beginning at 00H (00, 08, 10, 18, 20, . . . F0, F8).
Eight contiquous I/O addresses used; selection between translation and access registers by MSB of I/O data.

I/O ADDRESS FORMAT (EACH PORT)

AAAA A***

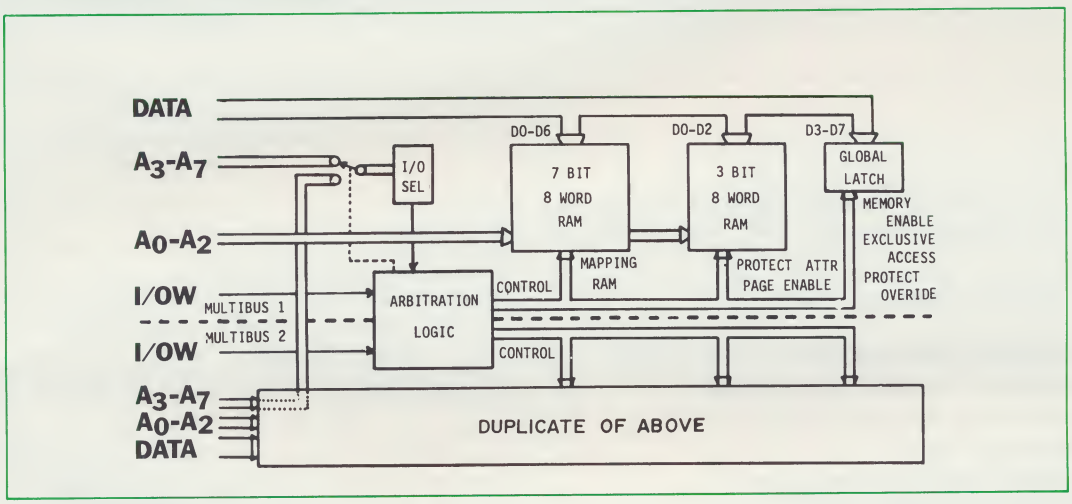
Strapped I/O base address	000	Register 0	Translation or Access Register to be written
	001	1	
	010	2	
	011	3	
	100	4	
	101	5	
	110	6	
	111	7	

I/O DATA FORMAT (EACH PORT)



Access commands which affect all banks may be written to any of the I/O addresses.

I/O SYSTEM — PICTORAL



INTERRUPTS

Occurs whenever a master port attempts access of memory protected by other port on write and/or read. Strap to any one of eight interrupt request lines for each port.

INTERFACES

Bus: all signals TTL-compatible.
Ports: Two identical MULTIBUS-compatible master ports; one slave address port for external memory.

CONNECTORS

INTERFACE,	NO. OF PINS	CENTERS (IN.)	MATING CONNECTORS
PORT A	86	0.156	CDC VPB01E43A00A1
PORT B	2 x 50	0.200	3M 3415-0001
Memory	60	0.100	CDC VPB01B30D00A1

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.5 cm)
Height: 6.75 in. ref. (17.1 cm)
Depth: 0.5 in. max. (13 mm)
Weight: 14 oz. (400 g.)

ELECTRICAL CHARACTERISTICS

DC Power (voltage ±5% tolerance)
+5 volts, 5 amperes nom.

ENVIRONMENTAL

Temperature
Operating: 0 to 55°C (32 to 131°F)
Storage: -40 to 100°C (-40 to 212°F)

BUS DESCRIPTION

See Intel Applications Note AP-28.

MEMORY SYSTEM

OUTPUT ADDRESS BUS — 20-bit address for both an onboard memory and an external "slave" bus. External bus provided at auxiliary MULTIBUS edge-connector, for address and data access to read/write and read-only memory on other modules (such as CM-118)

INPUT ADDRESS (two ports) — Either of two master MULTIBUS ports (as selected by contention-resolving logic). One port provided as a standard MULTIBUS connector, other as two 50-pin edge connectors at opposite edge of module. Either port can be strapped to 16 or 20-bit addresses.

ADDRESS TRANSLATION

20-Bit Master Port Address: Propagates to output bus as asserted; directly accesses 1 megabyte of memory.

16-Bit Master Port Address: 3 MSB of address select one of eight address translation registers; 13 LSB passed to output bus. Content of selected register forms 7 MSB of 20-bit effective address. Address space is accessed as 128 8K memory banks, with translation registers for eight 8K banks (total 65K) provided for each port.

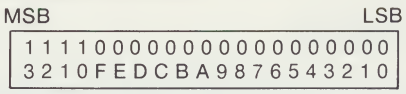
ONBOARD MEMORY — 16K static read/write; address strapped anywhere on a 16K boundary within 20-bit memory space.

ACCESS TIME

Either port: 350 to 420 ns (assuming no access by other port)
Alternate port: 350 to 420 ns, after granted bus
Two ports: 700 to 840 ns, on alternating basis
Times shown assume no wait states asserted by external memory; timeout of 1.5 to 2 μs ends access cycle if no acknowledge received from memory.

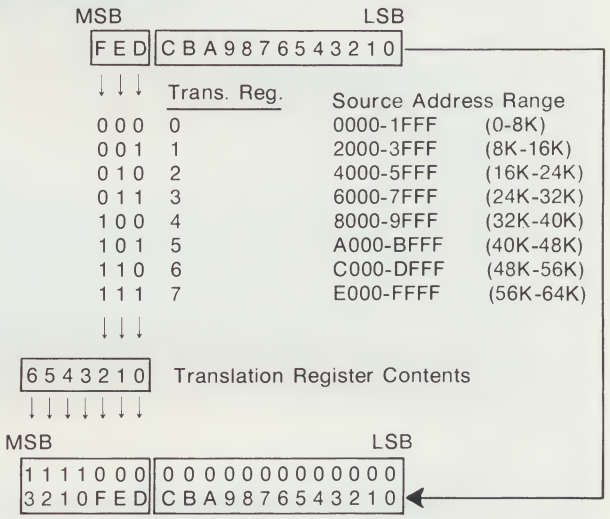
ADDRESS FORMAT

20-BIT BUS ADDRESS



Memory same as above (no translation)

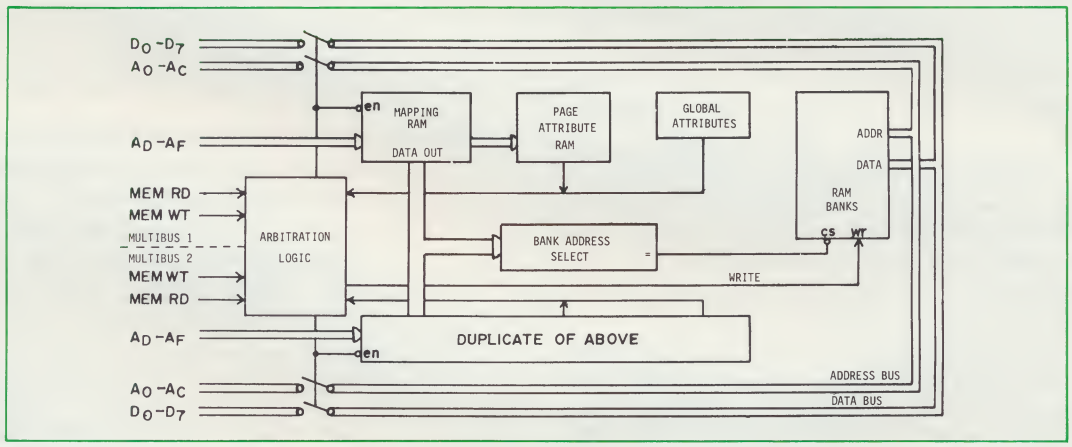
16-BIT MASTER PORT



Memory receives above composite 20-bit address.

Eight 7-bit translation registers for each master port. Translation register content (mapped address) modified by I/O write operations.

MEMORY SYSTEM — PICTORAL



RM-117 allows two identical MULTIBUS-compatible "master" ports to share a common memory area. Contention-resolving logic switches both address and data paths to the selected port. If one port requests memory access while the other port is being serviced, RM-117 delays its access until the current service is concluded.

RM-117 provides a full 20-bit (1 megabyte) address bus, which services both onboard 16K read-write memory and external expansion memory modules. An 8-bit data path is provided.

A master port may provide either a 16- or 20-bit address, as selected by strap option. If a 20-bit address is asserted, it propogates unchanged to the slave address bus.

If a master port is strapped for 16-bit addresses, RM-117 generates a composite 20-bit slave address whenever it accesses the bus. The 3 MSB of the master address select one of eight 7-bit translation registers; the contents of the selected register form the 7 MSB of the slave address. The 13 LSB of the master address pass directly to the slave bus to complete the 20-bit address.

Because each master port has its own set of address translation registers, it can uniquely map a common memory into eight 8K banks anywhere within a 1 megabyte range. Each master port can modify its effective slave address by using I/O write commands to its translation registers. In the same way, a master port can restrict access by the other port on memory read and/or write to any or all memory banks.

PROGRAMMING NOTES

GENERAL

Each MULTIBUS-compatible master port requires its own setup sequence, using standard output commands. Refer to "I/O Address Format" and "I/O Data Format" on page 2.

Eight contiguous I/O addresses are provided for each port. The MSB of the data byte directs the LSB seven bits of the value into either an address translation register or an attribute latch. Thus, each I/O address implies two seven-bit values.

Three bits of each attribute data byte are unique to (that is, paired with) a specific address translation register at the same I/O address. Three other bits are general to the port, and may be altered by a write to any of the eight I/O addresses. One bit is unused.

Note that all I/O operations are write-only, and no read verification of values is possible.

INITIAL CONDITIONS

Master Port Enable, which enables all activities of a port, is disabled on power clear or system reset. Address translation registers and other attributes contain arbitrary values. RM-117 translation and attribute bits should thus be written before the port is enabled.

ADDRESS REGISTER AND ATTRIBUTE SETUP

Refer to "16-bit Bus Address", page 3. If a 20-bit bus address is provided by the port, translation is not required.

A 16-bit source address is translated into a 20-bit address in 8K segments. The 3 LSB of the I/O address select the same eight translation registers on write as do the 3 MSB of the 16-bit address. The seven-bit register contents written by I/O command at setup are read at memory access time as the seven MSB of a 20-bit composite address.

1. Fetch the 7-bit translation value for the first translation register to be used. Set the MSB bit (bit 7) to zero, to allow translation register access. The data format is: 0AAA AAAA BINARY, where AAA AAAA are the seven MSB of the 20-bit translated address. For example, if the 20-bit address is to be in the range FC000 to FDFFF HEX, use the value 0111 1110 BINARY.
2. Write the value to the RM-117, using OUT NNNN NRRR BINARY, where NNNN N is the I/O base address (strap-selected) and RRR is the register desired, 0 to 7. For example, if a value for the source address range 2000-3FFF HEX is being written, use address NNNN N001 BINARY.
3. Fetch the 3-bit attribute pattern for the same port accessed in Step 2. (These are: WRITE PROTECT, READ PROTECT, and PAGE ENABLE.) The data format is: 1000 0AAA BINARY, where the MSB (bit 7) is one, selecting attribute register access, and AAA are the three attribute bits.
4. Repeat Steps 1 through 4 for each of the eight translation ranges to be used. (But see Global Command Setup, below.)

GLOBAL COMMAND SETUP

Global commands control overall port functions. These three bits are: PROTECT OVERRIDE, EXCLUSIVE ACCESS and MEMORY ENABLE. Because MEMORY ENABLE immediately activates the entire port, it should be set only after all translation and attribute data are written.

Global attributes may be written to any one of the eight I/O addresses, with the same results. However, because globals share the same data word with register-specific attribute bits, they should be combined with them; otherwise the attribute bits may be reset. Alternately, globals may be written to an I/O address corresponding to an unused translation register.

1a. For the last attribute write of Step 5 (above), combine the pattern of address-specific attributes with the desired global bits. Data format becomes: 1GGG 0AAA BINARY, where 1 selects attribute access, GGG are the global bits, and AAA are the attribute bits for the last port; or:

1b. Write the global bit pattern to an unused translation group. The data format is: 1GGG 0000, where the translation page remains disabled.

TRANSLATION ADDRESS MODIFICATION

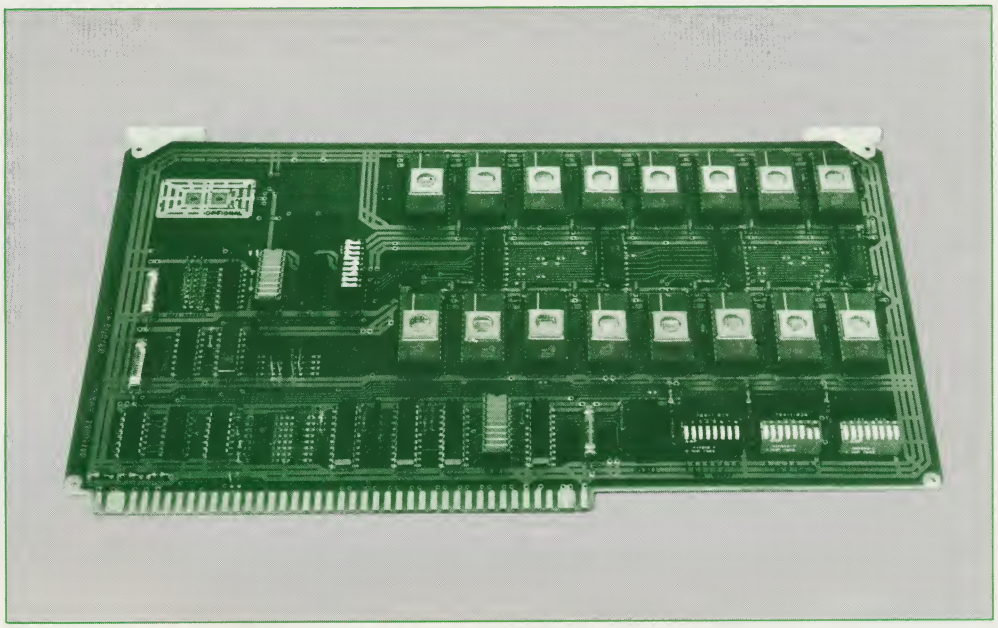
Translation addresses may be modified at any time during program operation.

1. Write the new translation value to the I/O address of the desired translation register. Data format is: 0AAA AAAA BINARY, where 0 allows translation register access and AAA AAAA is the translation value.
2. Write a new attribute byte to the same I/O address as Step 1. (This step is not required unless attributes must be changed.) Data format is: 1GGG 0AAA BINARY, where 1 selects attribute register access, GGG are the current global attributes desired for the entire port, and AAA are the register-specific attribute bits.

PRINTED IN U.S.A./RM-117. R0 7903-5M (DAY)

DATACUBE

DataRom
MODEL PM-116
16K-32K-64K PROM MEMORY



DataRom—a total PROM/ROM memory module for the Intel MULTIBUS™ . Provides over one megabits of read-only memory storage for Intel SBC/NSC BLC single-board computers. Accepts erasable and fusible-link PROMs and masked ROMs in all present 24-pin standard and future proposed formats, from 1K x 8 to 8K x 8 bits. Data are selected by a 16-bit (optional 20-bit) address and are presented on the bus as either 8 or 16-bit words.

- Intel MULTIBUS™ and NSC Compatible
- Each Device Individually Switch-Enabled
- PROMs Can Overlap Read/Write Memory
- 16-Bit Address Bus
  Expands to 20 Bits—option
- Data Word Selectable 8 or 16 Bits
- On-Board -5V Regulator
  (Optional—for Intel MDS-800)
- High-Reliability Side-Grip Sockets—
  Deep Pin Ramps for Easy Insertion
- Sixteen 24-pin Dip Sockets—
  Accept Present and Future Devices
- Selectable Access Time Delay for
  Slower Devices
- Independent Base Address for
  Each Memory Bank

DataRom from DATACUBE offers you full read-only memory functions for both current and next generation microcomputer system products. You can use today's standard 2708 PROMs—and tomorrow's 64K devices. Use DataRom in present 8080-type systems—and convert quickly to 20-bit address/16-bit data structures for new products, such as Intel's 8086.

DataRom accepts a wide variety of PROM/ROM devices, from older EPROMs to fast bipolar masked ROMs, by providing a selectable access time delay.

For use with the Intel MDS-800, a -5V regulator is available as an option.

DATACUBE SMK INC. ● 670 MAIN STREET ● READING, MA 01867 ● 617/944-4600 ● TWX-710-393-0144

SPECIFICATIONS

MEMORY ADDRESSING

Address bus standard 16 bits. Available option converts to 20 bits for memory paging.

Two banks of eight sockets each; each bank independently selectable memory boundary (see table of compatible devices).

Each pair of sockets can overlap read-write memory elsewhere on the bus; requires INH2 from read-write memory; generates INH1.

Each socket individually enabled; disabled device will not generate acknowledgement to bus access.

Address selection and device enable by means of dip slide switches.

DEVICE COMPATIBILITY

Accepts industry-standard 24-pin ROM and/or PROM devices. Jumper-plug selection to accommodate variations in pinout. See table of compatible devices.

DATA WORD SIZE

Eight or sixteen bits, jumper-selectable.

A single device provides 8-bit data; when 16-bit data are chosen, a pair of devices is accessed simultaneously.

BUS DESCRIPTION

All signals TTL-compatible.

See Intel Applications Note AP-28

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.5 cm.)
Height: 6.75 in. ref. (17.1 cm.)
Depth: 0.50 in. max. (13 mm.), less user-provided devices
Weight: 12 oz. (350 g.)

ELECTRICAL CHARACTERISTICS

DC Power: (all voltages ± 5% tolerance)
+5 volts, 1 ampere
+12 volts, −5 volts } Not required by DataRom; for user devices only.
Option: −5V derived from −10V (MDS-800)

Currents shown are for unloaded board; add current of installed user devices for total.

ENVIRONMENTAL

Temperature:
Operating: 0 to 55°C (32 to 131°F)
Storage: -40 to 100°C (-40 to 212°F)

COMPATIBLE DEVICES (partial listing)

DEVICE BYTES, EACH	1K	2K	4K*	8K*
BASE ADDRESS BOUNDARY— EACH BANK	8K	16K	32K	64K
MAX. STORAGE AVAILABLE— BYTES	16K	32K	64K	128K
EPROMs	2708 EA2708 MC2708 MC27A08 TMS2708 MB8518	TMS2516 2716 TMS2716	TMS2532 2732	
FIELD-PROGRAMMABLE PROMs	2608 MM6381 MM6385 DM77S288 DM87S288 93451	2616 82S191		
MASKED ROMs	2308 2607 TMS4700 MM6281 9208 DM85S28 93464 MK30000	2316E 2616 MM6276 MK34000	2632 TMS4742	2664

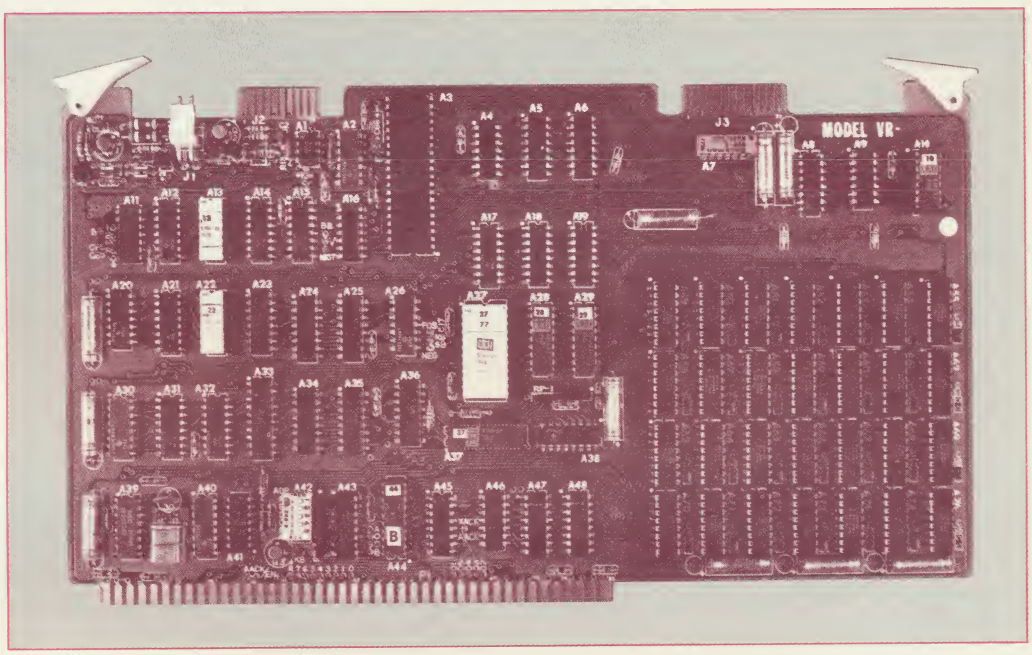
*These devices require optional jumper plug assembly.

Printed in U.S.A./PM-116, R0 7807-5M (DAY)

DATACUBE SMK INC. ● 670 MAIN STREET ● READING, MA 01867

DATACUBE

VideoRam
MODEL VR-110



VideoRam—a versatile series of video display modules for the Intel MULTIBUS™. Generate memory-mapped raster-scan display output for Intel SBC/NSC BLC single-board computers. Provide full program selection among four screen formats, to display as many as 1024 characters from a 128-character font in any combination of normal, reverse, half-intensity blink and underline modes. Mixed graphics, a flashing addressable cursor and an interrupt-driven keyboard port allow complete system applications.

Straight binary screen addressing and a 7x9 character matrix are provided.

- INTEL MULTIBUS™ & NSC Compatible
- Memory-mapped characters and graphics
- Screen Format:
  - 7x9 dot matrix display
  - binary addressing
- Programmable Display format
- Dual Video Outputs
  - direct (X-Y) drive
  - composite video
- Prom Character Generator — 128 Characters
- Directly-addressed Flashing Cursor
- Overlaid Character/Attribute Memory for:
  Any Combination of:
  - Regular or reverse video
  - Underline
  - Half-intensity
  - Blink
- Memory-Mapped Control and Keyboard Ports
- Memory Base Address on any 2K Boundary
- Full Screen Attribute Enable and Blanking

Because every character position is a separate location in main memory, your computer program can selectively write (and read) any of the 1024 positions in the display. A separate, overlaid memory provides the same access for four display attributes for each position.

These powerful capabilities allow you to easily program special displays — split-screen, text/command, text/directory and scrolling.

If you require a custom character display font, simply change the on-board plug-in ROM.

Three unique memory locations allow direct program control of all module functions, including screen format, blanking, and display attribute latching and enabling. A fourth location serves as data input port for an external keyboard.

Add your composite video or X-Y drive video monitor and a keyboard for a complete video terminal system.

DATACUBE SMK INC. • 670 MAIN STREET • READING, MA 01867 • 617/944-4600

BASIC FEATURES

COMPATIBILITY: Intel MULTIBUS™ (SBC-80 computer series);
National Semiconductor BLC-80 series
CHARACTERS/LINE: 64 or 32, program-selectable
CHARACTER LINES: 16 or 8, program-selectable
CHARACTERS: | program-selectable for each of 1024 screen positions
CURSOR (addressable): program-selectable for any one screen position
BLINK RATE: 1, 2, 4 or 8 Hz, strap selected
DISPLAY ATTRIBUTES — CHARACTERS
REVERSE VIDEO (B-O-W)
HALF-INTENSITY
UNDERLINE
BLINK
} Program-selectable for each of 1024 max. screen positions (characters only) and enabled individually for entire screen.
BLINK RATE: 1, 2, 4, or 8 Hz, strap selected
VERTICAL FREQUENCY: 60 Hz (50 Hz optional)
PERIOD: 16.7 msec.
COMPOSITE VIDEO LEVELS (75-ohm termination)

SYNC	0.0 Volts
BLANK	0.4
BLACK	0.5
HALF-INTENSITY	1.0
WHITE	1.5

DIRECT DRIVE (X-Y) COMPATIBILITY
Most popular video data displays, including:
BALL BOTHERS, Models TV-5, TV-9, TV-12, TV-120
MOTOROLA, Models M-1000. M-2000, M-3000, M-4000

ADDRESSING FORMAT	BINARY
MEMORY SPACE	2048
CHARACTER MATRIX (HxV)	7x9
BLOCK	9x15
TIMING-HORIZONTAL	
HORIZONTAL FREQ. (KHz)	15.72
PERIOD (usec)	63.61
DLY BEFORE SYNC	1.59
SYNC	4.77
DLY AFTER SYNC	6.36
BLANKING	12.72
DRIVE (BALL BROS.)	28.6
MOTOROLA	4.77
TIMING-VERTICAL	
DELAY BEFORE SYNC (usec)	191
SYNC (usec)	191
DELAY AFTER SYNC (usec)	954
BLANKING (msec)	1.4
DRIVE (BALL BROS.) (msec)	1.4
(MOTOROLA) (usec)	191

OPTIONS

ALTERNATE CHARACTER FONTS (special order)
VERTICAL FREQUENCY: 50 Hz (special order)

CABLE ASSEMBLIES (all 3ft. — 1M)	PART NO.
KEYBOARD PORT RIBBON CABLE, CONNECTOR	C-10001
DIRECT DRIVE RIBBON CABLE, CONNECTOR (for Ball Bros. or Motorola monitor)	C-10002
COMPOSITE VIDEO CABLE, CONNECTOR	C-10003

KEYBOARD ASSEMBLY (Models SMK 53, 62, 73 and 86)
ASCII-encoded, 53 to 86-key, w/cable, connectors
Solid/state capacitive-key, N-Key rollover

Give Your Present CPU Video I/O Capability

This Board Makes Real Time Digitized Imaging Possible... Economically

Put sight in your present system. It's as simple as mating your computer with one of the VG-120 Video Graphics boards from Datacube. Our boards can digitize and display information from standard video cameras and CRT's for Intel's MULTIBUS™ and DEC's Q-BUS™ systems.

The VG-120 boards couple easily to your system; inputs and outputs are EIA-compatible (RS-170 and RS-420) with up to 8 bits A/D and D/A outputs. Our boards digitize data at 5 million pixels per second, and they provide video output from digitized information at 5 million pixels per second — all without computer intervention.

Besides providing binary storage, these boards can generate video from memory for monitors, recorders, and telecommunications. They store up to 320 H x 256 V x 8 bits in 256 luminance levels with higher resolutions available upon request.

Pseudo-color and black-and-white versions of the VG-120 are available.

And what will it cost to bring sight to your present system? As little as 3,000. Call Datacube today for specific price information and full technical details.

Datacube

670 Main St., Reading, MA 01867

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Datacube Inc.

MANUFACTURER OF Q BUS AND MULTIBUS:

B/W & Color Video Control

Alphanumerics
Format: 64 X 16, 80 X 24, 128 X 48

Graphics
Resolution: 320 X 256 X 8
640 X 512 X 4
768 X 512 X 8

Real-Time Image Processing

Image Digitizer
Video ALU Feedback Processor
Resolution: 768 X 512 X 8-16

Memory Storage

32K Statics RAM
64K Dynamic RAM
128K Dynamic RAM

Dual Port RAM

OEM PROM / EPROM Board

Datacube
670 Main St., Reading, MA 01867
Telephone (617) 944-4600 TWX 710-393-0144

Price List

Video Graphic Boards

April 1981

For INTEL MULTIBUS™

Model	Description	1-9	10-24
VG-120A	**320 x 240 x 6, B & W, No Input Module**	$2495.00	$2300.00
VG-120B	**320 x 240 x 6, B & W, With Input Module**	2995.00	2760.00
VG-120C	**320 x 240 x 6, Color, No Input Module**	2595.00	2400.00
VG-120D	**320 x 240 x 6, Color, With Input Module**	3195.00	2945.00
VG-120E	**320 x 240 x 3 Bits, Red, Green, Blue**	1500.00	1380.00
VG-120E/S	**320 x 240 x 3, VG-120E with Scroll**	1600.00	1475.00

Model	Description	1-9	10-24
VG-220A	**640 x 240 x 3 Bit, B & W Output**	$2495.00	$2300.00
VG-220B	**640 x 240 x 3 Bit, B & W Input & Output**	2995.00	2760.00
VG-220C	**640 x 240 x 3 Bit, Red, Green, Blue Output**	2595.00	2400.00
C-10005	**Video Connector Package for VG-120, VG-220, QAF-120**	25.00	23.00
C-10006	**Cable Set for VG-120, VG-220, QAF-120**	50.00	46.00
VG-120D PROM	**Color Prom — One Time Setup Charge**	200.00	—

For DEC LSI 11 Q-BUS

Model	Description	1-9	10-24
QVG-120	**320 x 240 x 8, No Input Module**	$2895.00	$2670.00
QVG-120A	**320 x 240 x 8, With 8 Bit B & W Output**	2995.00	2760.00
QAF-120-X-Y	**Analog Front End for QVG-120 (LUT = Look Up Table)**	Y = Number of 8 Bit D/A X = Bits of A/D	
QAF-120-8-1	**8 Bit A/D, with Input LUT, 8 Bit D/A with Output LUT**	2495.00	2300.00
QAF-120-8-3	**8 Bit A/D, with Input LUT, 3 x (8 Bit D/A with Output LUT)**	2895.00	2670.00
QAF-120-6-1	**6 Bit A/D, with Input LUT, 8 Bit D/A with Output LUT**	1595.00	1470.00

Model	Description	1-9	10-24
QAF-120-6-3	**6 Bit A/D, with Input LUT, 3 x (8 Bit D/A with Output LUT)**	$1995.00	$1840.00
QAF-120-4-1	**4 Bit A/D, with Input LUT, 8 Bit D/A with Output LUT**	1450.00	1340.00
QAF-120-4-3	**4 Bit A/D, with Input LUT, 3 x (8 Bit D/A with Output LUT)**	1850.00	1695.00
QAF-120-0-1	**No Input, 8 Bit D/A with Output LUT**	1350.00	1240.00
QAF-120-0-3	**No Input, 3 x (8 Bit D/A with Output LUT)**	1750.00	1610.00

ROM PROM RAM

Model	Description	1-9	10-24
CM-126A	**80 ns to 800 ns Mix Prom, Ram, and Rom**	$695.00	$595.00

Model	Description	1-9	10-24
CM-126 PROGRAM	**Prom Setup for CM-126, Speed & Memory Map (one time)**	$100.00	—

Alpha/Numeric

Model	Description	1-9	10-24
VT-103A or B	**64 x 16 Character I/O Map**	$495.00	$410.00
VT-103BP	**64 x 16 Character I/O Map Phase Lock**	520.00	435.00
VR-107A	**80 x 24 Character 160 x 120 Graphics Memory Mapped**	540.00	495.00
VR-109A	**80 x 24 Character 160 x 144 Graphics Memory Mapped**	560.00	510.00
VR-110A	**64 x 16 Character to 32 x 8 Character Memory Mapped**	450.00	395.00

Model	Description	1-9	10-24
CUSTOM FONT	**One Time Charge per Font**	$100.00	—
C-10001	**Keyboard Port Ribbon Cable, Connector**	25.00	25.00
C-10002	**Direct Drive Ribbon Cable, Connector**	25.00	25.00
C-10003	**Composite Video Cable, Connector**	16.00	16.00

Dynamic RAM

Model	Description	1-9	10-24
RM-119-016	**16 K x 8 Bit 350 ns Access 550 ns Cycle**	$575.00	$529.00
RM-119-032	**32 K x 8 Bit**	599.00	551.00

Model	Description	1-9	10-24
RM-119-048	**48 K x 8 Bit**	$624.00	$574.00
RM-119-064	**64 K x 8 Bit**	649.00	597.00

Dual Port RAM

Model	Description	1-9	10-24
EM-115-016	**Dual Port expansion 16 K 400 ns/800 ns**	$650.00	$535.00
EM-115UP	**Dual Port Expansion Board**	195.00	160.00

Model	Description	1-9	10-24
RM-117	**Dual Port Memory Board 400 ns/800 ns**	$1200.00	$995.00

Static RAM

Model	Description	1-9	10-24
CM-118	**32 K 250 ns**	$810.00	$810.00
CM-118SL	**32 K 450 ns**	760.00	760.00

Model	Description	1-9	10-24
CM-118-16SL	**16 K 450 ns**	$655.00	$655.00

4 Channel Color

Model	Description	1-9	10-24
VS-130	**Scrolling Strip Chart Recorder Board**	$430.00	$395.00

PROM

Model	Description	1-9	10-24
PM-116	**Prom Board Up to 64 K x 8 Bit**	$265.00	$220.00

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Date: APRIL 1981
Contact: ROBERT WANG
MARKETING MANAGER

For Release: IMMEDIATE

News Release

VR-111

HIGH RESOLUTION COLOR VIDEO, ALPHANUMERIC, AND GRAPHIC CONTROLLER

READING, MASSACHUSETTS, APRIL 1981 - - - DATACUBE, INC., A MANUFACTURER OF THE STATE OF ART VIDEO PRODUCT, IS PLEASED TO INTRODUCE THE VR-111, A PROGRAMMABLE HIGH-RESOLUTION COLOR ALPHANUMERIC AND GRAPHIC CONTROLLER. THE VR-111 IS A SINGLE STAND ALONE BOARD THAT EASILY INTERFACES WITH BOTH THE INTEL MULTIBUS AND THE DEC Q-BUS.

THE VR-111 CAN DISPLAY SIMULTANEOUSLY BOTH COMPUTER GENERATED COLOR ALPHANUMERIC UP TO 128 CHARACTERS BY 48 LINES, AND COLOR GRAPHIC PLANES AT RESOLUTIONS OF 768 X 512 MATRIX, WITH 8 COLORS PER PIXEL. BOTH ALPHANUMERICS AND GRAPHICS ARE OVER-LAYED ON THE DISPLAY SCREEN. FULL HORIZONTAL PANNING AND VERTICAL SCROLLING OF THE GRAPHIC DISPLAY BY DOT, AND ALPHANUMERIC BY CHARACTER. MULTIPLE TEXT ATTRIBUTES AND PROGRAMMABLE CHARACTER SET CAPABILITIES. THE COMBINATION ALPHA/GRAPHIC APPLICATIONS OF THE VR-111 INCLUDE INDUSTRIAL PROCESS CONTROL DISPLAY, INSTRUMENTATION CONTROL DISPLAY, MANAGEMENT GRAPHICS, COLOR WORD PROCESSOR, FOREIGN TEXT DISPLAY, AND MANY OTHERS.

DATACUBE, INC. NEWS RELEASE APRIL 1981

GENERAL SPECIFICATION: STANDARD: RS-170, 330

GENLOCK: TO RS-170, 330, MASTER/SLAVE

VIDEO OUTPUT: COMP VIDEO/RGB (TTL ANALOG), H & V SYNC/DRIVE

ALPHANUMERIC:

PROGRAMMABLE

FORMAT: FROM 16 TO 128 CHARACTERS PER LINE AND FROM 8 TO 48 LINES PER DISPLAY

CHARACTER CELL MATRIX: HORIZONTAL 5,6,7,8,9,10,12,14,16 DOTS PER LINE
VERTICAL 1 - 16 LINES

STORAGE: UP TO 8K BYTE TEXT AND 8K BYTE ATTRIBUTE

ATTRIBUTES AVAILABLE: FOREGROUND/BACKGROUND WITH 8 COLORS EACH
FOREGROUND OR BACKGROUND WITH BLINK
INVERT, UNDERLINE, DOUBLE HEIGHT, DOUBLE WIDTH, AND BOLD FACE

CHARACTER GENERATOR: 2716 PROM
PROGRAMMABLE 2K BYTE RAM
TOTAL 4K BYTE OF CHARACTER GENERATOR STORAGE

ADDRESSING: I/O MAPPED CONTROL REGISTERS
BANK SELECT MEMORY MAPPED DISPLAY

SCREEN MANIPULATION: SCROLL AND PAN BY CHARACTERS

DATA TRANSFER RATE: FROM 2 - 5 MEGA BYTE PER SECOND

GRAPHIC:

RESOLUTION: 768 X 512 X 3, 8 COLORS, RGB
OR 2 PAGE OF 384 X 256 X 3

ADDRESSING: X Y INDIRECT I/O MAPPED REGISTERS

SCREEN MANIPULATION: SCROLL AND PAN BY DOT

DATA TRANSFER: AUTO INCREMENT AND DECREMENT ADDRESS AND VECTOR PLOTTING CAPABILITY

DATA TRANSFER RATE: 1.20 MEGA BYTE PER SECOND

PHYSICAL DIMENSION: ONE 6.75" X 12" MULTIBUS BOARD

AVAILABILITY: 3RD QUARTER 1981

PRICE: VR-111 ALPHA - QTY. 1 TO 9, $799.
VR-111 GRAPHIC - QTY. 1 TO 9, $1899.
VR-111 ALPHA & GRAPHIC - QTY. 1 TO 9, $2599.

670 Main st. Box 405 Reading, Ma. 01867 (617) 944-4600

Datacube INC.
670 Main St., Reading, MA 01867
Telephone: (617) 944-4600 TWX 710-393-0144

Date: MAY 1981
Contact: ROBERT WANG
MARKETING MANAGER

For Release: IMMEDIATE

News Release

VP-122 - MULTIBUS
QVP-122 - Q-BUS

REAL TIME DIGITAL VIDEO PROCESSOR

READING, MASSACHUSETTS, MAY 1981, - - - DATACUBE, INC., A MANUFACTURER OF THE STATE OF ART VIDEO CONTROLLER FOR THE INTEL MULTIBUS AND THE DEC Q-BUS, IS PLEASED TO INTRODUCE THE Q/VP-122.

THE Q/VP-122 PROCESSES VIDEO IMAGES IN REAL TIME WITH FULL SPATIAL RESOLUTION OF 768 X 512 AND AMPLITUDE RESOLUTION OF 256 LEVELS. AN ENTIRE FRAME OF VIDEO DATA IS DIGITIZED STORED ON BOARD FOR VIDEO OR CPU PROCESSING. THE THROUGH PUT OF THE Q/VP-122 IS AT 14 MIPS (14 MILLION INSTRUCTIONS PER SECOND) WHICH IS NOT ATTAINABLE VIA CONVENTIONAL SOFTWARE TECHNIQUES. THE ADDED INTELLIGENCE OF THE Q/VP-122 FACILITATES PIPE LINE PROCESSING, IMAGE AVERAGING, IMAGE NOISE REDUCTION, EDGE ENHANCEMENT, CORRELATION AND CONVOLUTION OF REAL TIME VIDEO IMAGERY DATA.

THE TYPICAL APPLICATION OF Q/VP-122 INCLUDES:

- LANDSAT AND REMOTE SENSING IMAGE ANALYSIS
- ASTRONOMY
- INDUSTRIAL RADIOGRAPHY
- ROBOTIC PATTERN RECOGNITIONS
- OPTICAL/ELECTRON MICROSCOPY
- PRODUCT INSPECTION, INFARED AND VISABLE
- MEDICAL FLUOROSCOPY
- SURVEILLANCE
- CAD LINE DRAWING DIGITIZING
- IMAGE TRANSMISSION
- COMPUTER GRAPHICS

THE Q/VP-122 EASILY INTERFACES TO THE DEC LSI Q-BUS (11/23) AND THE INTEL MULTIBUS (8086/Z800).

DATACUBE, INC. NEWS RELEASE MAY 1981

SPECIFICATIONS:

SPATIAL RESOLUTION: 768 X 512 X 8 BY 1 PAGE
384 X 512 X 8 BY 2 PAGE

AMPLITUDE RESOLUTION: 8 BIT/PIXEL, 256 GREY LEVEL OR PSEUDO COLOR OUT OF 16 MILLION COMBINATIONS

SCREEN MANIPULATION: CURSOR, CROSS HAIR
SCROLL AND PAN BY DOT
HARDWARE CLIPPING AT END OF LINE OR END OF FIELD

PIXEL DEPTH: MULTIPLE Q/VP-122 CAN BE STACKED TO OBTAIN 24 BITS/PIXEL OR MORE (RGB)

DATA TRANSFER RATE TO CPU: 1.25 MEGA BYTE TYPICAL

ARITHMATIC FUNCTION FOR VIDEO PROCESSING: ADDITION, SUBTRACTION, AND, OR, XOR
THROUGH PUT AT 14 MIPS

MULTIPLE BINARY IMAGE: UP TO 8 PLANES OF BINARY IMAGE OF 768 X 512 X 1 CAN BE INDIVIDUALLY STORED AND RETRIEVED PER VP-122

VIDEO INPUT: RS-170, DIGITIZE AT 4X COLOR BURST RATE
8 BIT FLASH A/D WITH TRANSFORMATION TABLE
AGC & DC RESTORATION
SELECTABLE GAIN & OFFSET FOR GREY LEVEL ZOOM
GENLOCK CAPABILITY

VIDEO OUTPUT: RS-170
THREE 8 BIT D/A EACH WITH TRANSFORMATION TABLE
DRIVE B/W OR COLOR MONITOR

PHYSICAL: 6.75" X 12.00" X 2 MULTIBUS BOARDS
OR 8" X 10" X 2 DEC Q-BUS QUAD BOARDS

AVAILABILITY: 3RD QUARTER OF 1981

PRICE: $7,500. PER SET, QTY. 1 TO 9

670 Main st. Box 405 Reading, Ma. 01867 (617) 944-4600

Datacube INC.
670 Main St., Reading, MA 01867
Telephone: (617) 944-4600 TWX 710-393-0144

Date: MAY 1981
Contact: ROBERT WANG
MARKETING MANAGER
For Release: IMMEDIATE

News Release

QVG-120/QAF-120

NEW TEAM OF GRAPHICS AND MEMORY BOARDS FOR THE DEC LS11 QBUS

TOTAL VIDEO ACQUISITION AND DISPLAY ARE HANDLED BY THE QVG-120 AND QAF-120 DEC QBUS-COMPATIBLE TWO-BOARD TEAM. THEY ACQUIRE A FULL SCREEN OF DISPLAY INFORMATION FROM ANY EIA STANDARD VIDEO SOURCE, SIMULTANEOUSLY DIGITIZE AND STORE THE REAL-TIME DATA. IMAGE DATA ON THE QVG-120 CAN THEN BE PROCESSED BY THE CPU AND TRANSFERRED AT UP TO 1.25-MBYTE RATE. THE IMAGE DATA IS RECONSTRUCTED BY THE QAF-120 VIA A RAM OUTPUT LOOK-UP TABLE AND SENT TO D/A CONVERTERS THAT PRODUCE AN RS-170 STANDARD ANALOG SIGNAL TO DRIVE COLOR OR BLACK/WHITE MONITORS. AUTO-IMCREMENT SCREEN ADDRESS REGISTERS ENABLE EASY SEQUENTIAL DATA ACCESS.

THE QBUS-ORIENTED COMPUTER CAN EVALUATE AND MODIFY 6- OR 8-BIT VIDEO DATA FOR IN-PLACE ENHANCEMENT, AND GENERATE ITS OWN BINARY MEMORY PATTERN FOR DISPLAY AS VIDEO. THE COMPUTER CAN ALSO TRANSMIT THE SAME MEMORY INFORMATION TO A REMOTE SITE FOR DISPLAY OR ANALYSIS. APPLICATIONS INCLUDE PATTERN RECOGNITION, COMPUTER-GRAPHIC, THERMAL IMAGERY AND OTHERS.

HIGH-DENSITY VIDEO BINARY STORAGE AND REGENERATION USES 320 (H) BY 240 (V) PIXELS WITH 8-BIT RESOLUTION. DATACUBE, INC., 670 MAIN ST., READING, MASSACHUSETTS 01867, PRODUCES TWO OUTPUT VIDEO VERSIONS - BLACK AND WHITE WITH 256-LEVEL ILLUMINANCE, OR PSEUDOCOLOR WITH 256 COLOR SHADES OUT OF 16 MILLION POSSIBLE COMBINATIONS. AVERAGE ACCESS TIME IS 800NS.

THE INPUT SECTION CONSISTS OF AN EIA STANDARD VIDEO INPUT, REAL-TIME 8-BIT ADC, COMPUTER-CONTROLLED FRAME FREEZE, AND H-V OR COMPOSITE SYNC OUTPUTS, AND RGB VIDEO OUTPUTS. BUS AND VIDEO DRIVE SIGNALS ARE TTL-COMPATIBLE. VIDEO TIMING MEETS EIA SPEC RS-170, AND THE BOARD TEAM CAN BE CRYSTAL-CONTROLLED OR REFERENCED TO AN EXTERNAL TIMING SOURCE.

INDIRECT (X,Y) MEMORY ADDRESSING IS VIA HORIZONTAL AND VERTICAL ADDRESS PORTS. INDIRECT ADDRESSING WITH AN AUTO-INCREMENT MODE ENABLES A DATA TRANSFER RATE OF UP TO 1.2MBYTES/S. PORTS MAY BE ADDRESSED EITHER IN I/O OR IN MEMORY-MAPPED MODE.

SPECIFICATIONS:

QVG-120: RESOLUTION: 320 X 240 X 8 BITS/PIXEL

ADDRESSING: X, Y INDIRECT - OCCUPIES 8 CONSECUTIVE I/O PAGE BYTE LOCATIONS

DATA TRANSFER: AUTO ADDRESS INCREMENT UP TO 1.25 MEGABYTE RATE

VIDEO STANDARD: RS-170

VIDEO INPUT/OUTPUT: SEE QAF-120. GENLOCK CAPABILITY, EXTERNAL DRIVE FOR VIDEO CAMERA

POWER REQUIREMENT: +5, ±12

PHYSICAL DIMENSION: 8" X 10", ONE DEC QUAD SIZE

QAF-120: ADDRESSING: OCCUPIES 8 CONSECUTIVE BYTE LOCATIONS

VIDEO INPUT: 6 OR 8 BITS FLASH A/D WITH 1K BYTE INPUT BIPOLAR LOOK UP TABLE. AGC AND DC RESTORATION. PROGRAMMABLE GAIN FACILITATES AMPLITUDE ZOOM

VIDEO OUTPUT: UP TO 3 SEPARATE 8 BIT D/A EACH WITH 1K BYTE OUTPUT BIPOLAR LOOK UP TABLE. 256 LEVELS OF GREY SCALE OR COLOR SHADES OUT OF 16 MILLION COMBINATIONS

ADDITIONAL FEATURES: WIRE WRAP AREA PROVIDED

POWER REQUIREMENT: +5, ±12

PHYSICAL DIMENSION: 8" X 10", ONE DEC QUAD SIZE

DELIVERY: 2 TO 4 WEEKS, ARO

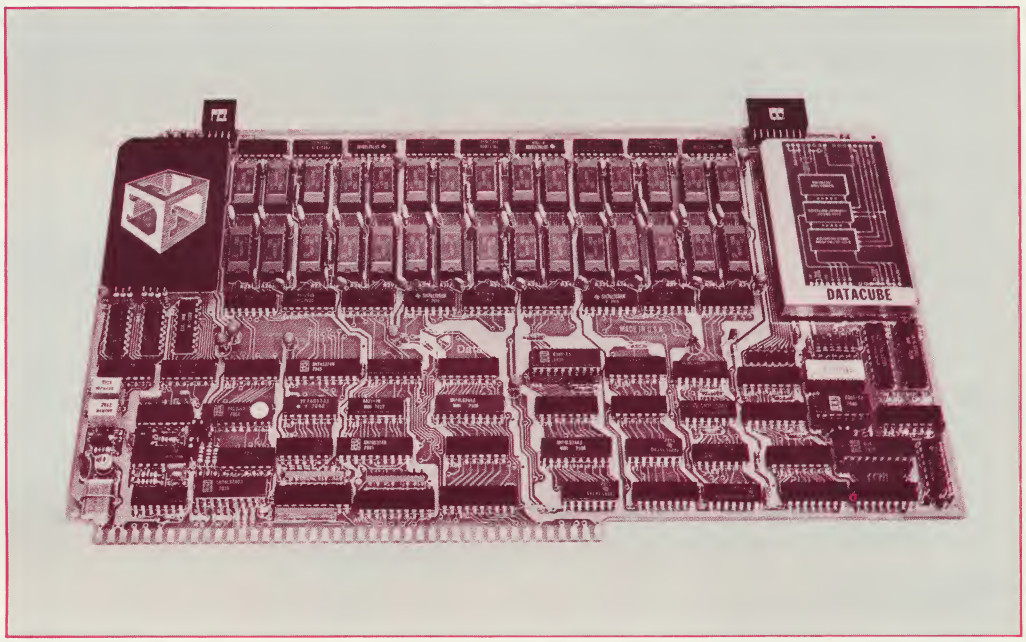
PRICE: $4,999. PER SET, QTY. 1 TO 9

IF YOU HAVE ANY QUESTIONS REGARDING TO THE ABOVE PRODUCTS, PLEASE CONTACT MR. ROBERT WANG, MARKETING MANAGER.

670 Main st. Box 405 Reading, Ma. 01867 (617) 944-4600

Datacube INC.

VIDEO GRAPHICS
MODELS VG-120/VG-220



A total video acquisition and display system for the Intel MULTIBUS™. Provides binary storage and regeneration of a full screen of video information.

Quality resolution of black-and-white or pseudo-color images. True EIA-compatible inputs and outputs. Full computer access of binary screen memory.

- **Intel MULTIBUS™ and NSC Compatible**
- **High-Density Video Binary Storage and Regeneration—**
  VG-120: 320H x 240V pixels (total 76,800)
  VG-220: 640H x 240V pixels (total 153,600)
  Both: optional 256V lines
- **High Pixel Resolution—Choose 3 or 6 Bits**
- **Full Computer Access to Storage—for Analysis, Enhancement, Remote Transmission**
- **Full EIA Specification Video—RS-170 (interlaced), or RS-420 (non-interlaced)**
- **Internal (crystal) or Gen-Lock Video Timing**
- **Four Basic Versions:**
  - **Black & White (8 or 64-level illuminance)**
  - **Pseudo-Color (8 or 64 color shades)**

INPUT SECTION (Optional)

- **EIA-standard Video Input**
- **Real-Time Flash A/D Converter—Choose 3 or 6 Bit Resolution**
- **Computer-Controlled Frame Grab**
- **Camera Drive Available—H-V and Composite Sync**

MEMORY

- **On-Board Full-Screen Binary Memory—245,760 to 491,520 Bits**
- **Computer Read/Write Access to Video Data**
- **Port-Type Memory Access—I/O or Memory-Mapped (16 or 20-Bit Bus)**
- **Address Auto Increment on Data Transfer**
- **X-Y (Indirect) Memory Addressing**

OUTPUT SECTION

- **Real-Time D/A Converter—Choose 3 or 6 Bit Resolution**
- **EIA-Standard Video Output**
- **H-V and Composite Sync Outputs**
- **Color (R-G-B) Video Output Option**

VG-120 and -220 can acquire a full screen of display information from any EIA-standard video source. The data, with 3 or 6-bit resolution, are then available in an on-board memory for computer access. Choose between 320 or 640 screen display locations (pixels) per line and 240 or 256 lines.

Your MULTIBUS-based computer can evaluate and modify video data for in-place enhancement and later display by the VG-120 or -220. Auto-increment screen address registers allow for easy sequential data access.

Instead of using external video, the computer can generate its own binary memory pattern for display.

VG-120 and -220 generate EIA-standard video from on-board memory for a television monitor, tape recorder or transmitter. Both black-and-white and pseudo-color display versions are available. And your computer can transmit the same memory information to a remote site for display or analysis.

DATACUBE INC. ● 670 MAIN STREET ● READING, MA 01867 ● 617/944-4600 TWX 710/393-0144

SPECIFICATIONS

MEMORY ADDRESSING

On-board binary memory, total 245,760 or 491,520 bits. See Screen Format.

Indirect (X-Y) addressing via horizontal and vertical vector ports. Automatic increment of memory address selectable for read or write access.

PORT ADDRESSING

Eight contiguous port addresses allocated—see Data and Control Ports.

Ports addressed either as I/O or memory locations on MULTIBUS (strap options).

I/O-mapped mode: strap to an I/O address on any 8-byte boundary; module decodes a full 12-bit I/O address.

Memory-mapped mode: strap to a memory address on any 8-byte boundary within a full 20-bit address range. Automatically compatible with 16-bit address bus; 4 MSB default to zero. Two inhibit outputs (INH1, INH2) available by strap options to provide for memory overlay.

INTERFACES

Composite Video: All signals EIA standards compatible—RS-170 (interlaced), or RS-420 (non-interlaced)

Video Drive: All signals TTL-compatible

External Sync Inputs: TTL-compatible with optional termination resistors (+5V, ground)

BUS DESCRIPTION

All signals TTL-Compatible

See Intel MULTIBUS Application Note AP-28A and IEEE Proposed Bus Specification 796.

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.5 cm.)
Height: 6.75 in. ref. (17.1 cm.)
Depth: 0.5 in. max. (13 mm.)
Weight: 20 oz. (570 g) approx.

ELECTRICAL CHARACTERISTICS

DC Power (all voltages ±5% tolerance):
+5 volts, 3 amperes
-5 volts, 0.1 ampere
+12 volts, 0.6 ampere
-12 volts, 0.3 ampere

ENVIRONMENTAL

Temperature:
Operating: 0 to 55° C (32 to 131° F)
Storage: -40 to 100° C (-40 to 212° F)
Humidity: 10 to 90% RH, non-condensing

CONNECTORS

INTERFACE	NO. OF PINS	CENTERS (in.)	MATING CONNECTORS
Bus	86	0.156	CDC VPB01E43A00A1
VIDEO			
Input	8	0.100	AMP 87631-4
Output	16	0.100	AMP 1-87631-2
Pin (F)			AMP 87045-2

SCREEN FORMAT

	H	V	Total Pixels	RS-170 Display Limit
VG-120	320	256	81,920	76,800 (240 lines)
VG-220	640	256	163,840	153,600 (240 lines)

MODEL SELECTIONS

All model designations begin with "VG—"

	320H			640H	
	6-Bit B&W	3-Bit R-G-B	6-Bit R-G-B	3-Bit B&W	3-Bit R-G-B
No Video Input	120A	120E*	120C	220A	220C
With Video Input	120B		120D	220B	220D

*Note: Available with scroll option; order as VG-120E/S.

OPTIONS

All versions:

Option 01: Extended vertical display—adds 16 lines at bottom of screen—from 240 to 256V. (Not compatible with EIA RS-170.)

Option 02: 50 Hz operation (625 raster lines—256V display (special order)

Versions -C and -D only:

Option 03: Custom color shade PROM—select 64 available shades from a choice of 2,048 colors and 32 saturation levels for each shade—a one-time set-up charge.

VIDEO TIMING

HORIZONTAL TIMING

	(60 Hz)	(50 Hz)
Horizontal Frequency (KHz)	15.750	15.625
Timing in microseconds:		
Period	63.5	64.0
Active Scan	52.1	51.2
Blanking	11.4	12.8
Front Porch	1.63	1.60
Sync	4.88	4.80
Back Porch	4.88	6.40
Equalizing	2.44	2.40
Field Sync	29.3	27.2
Horizontal Drive	6.35	6.40

VERTICAL TIMING

	60	50
Vertical Frequency (Hz)		
Timing in milliseconds:		
Period	16.7	20.0
Active	15.2	16.4
Equalizing	0.190	0.160
Sync	0.190	0.160
Blanking	1.43	1.61
Vertical Drive	0.571	0.576
Pixel Clock (MHz), VG-120	6.14	6.25
VG-220	12.28	12.5
Pixel Sampling Rate (nsec.), VG-120	163	160
VG-220	81.5	80
CPU Access Time (nsec. avg.)	814	800

DATA AND CONTROL PORTS

(X indicates unused bit)

Base Address +			READ 7 6 5 4 3 2 1 0	WRITE 7 6 5 4 3 2 1 0
0	**DATA PORT**	Three-bit models:	X X 2 1 0 2 1 0 (Right Pixel / Left Pixel)	X X 2 1 0 2 1 0 (Right Pixel / Left Pixel)
		Six-bit models:	X X 5 4 3 2 1 0	X X 5 4 3 2 1 0

NOTE: B&W models—64 illuminance levels, 0=black, 3F HEX=white
R-G-B models—64 color shades, PROM-selected

1 —RESERVED—

2 —RESERVED—

3 —COMMAND PORT—

READ: 7 6 X X 3 2 1 0 (see write)
- 1 = busy flag (1=busy)
- 0 = acquire flag

WRITE: X X X X 3 2 1 0 — Control—see tables

Access Control (of on-board video memory):

BIT 1	0	
0	0	computer access—no address increment
0	1	computer access—post increment on read
1	0	computer access—post increment on write
1	1	video input access (computer access blocked) (Command Port bit 7 = 1 until a full frame has been digitized.)

Display Control

Display memory value for all pixels as:

BIT 3	2	
		3-bit versions—no effect
		6-bit versions:
0	0	64 shades, color and intensity from PROM
0	1	16 shades from PROM, 4 intensities from memory
1	0	32 shades from PROM, LSB from memory is white
1	1	64 B&W levels from PROM, LSB from memory is black

		READ 7 6 5 4 3 2 1 0	WRITE 7 6 5 4 3 2 1 0
4	**H ADDRESS LO** horizontal address—8 LSB	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
5	**H ADDRESS HI**	X X X X X X X 0	X X X X X X X 0
6	**V ADDRESS**	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
7	**SCROLL (VG-120E/S only)** line offset from display memory base	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0

PROGRAMMING NOTES

INITIALIZE ROUTINE

Initialize Registers:

1. Write zero to: Command Port;
   H Address LO Port;
   H Address HI Port;
   V Address Port
   Scroll Port (if VG-120E/S)

Clear Screen:

2. Write 02 HEX to Command Port to select post-increment on write;
3. Write zero to Data Port 81,920 consecutive times to clear screen memory.

FRAME ACQUISITION

1. Write 03 HEX to Command Port to enable (video) acquire mode;
2. Write zero to Command Port to disable video acquisition (which takes effect after current frame is fully acquired);
3. Read Command Port bit 7 for done status (bit 7=1 if still busy).

REMOTE TRANSMISSION

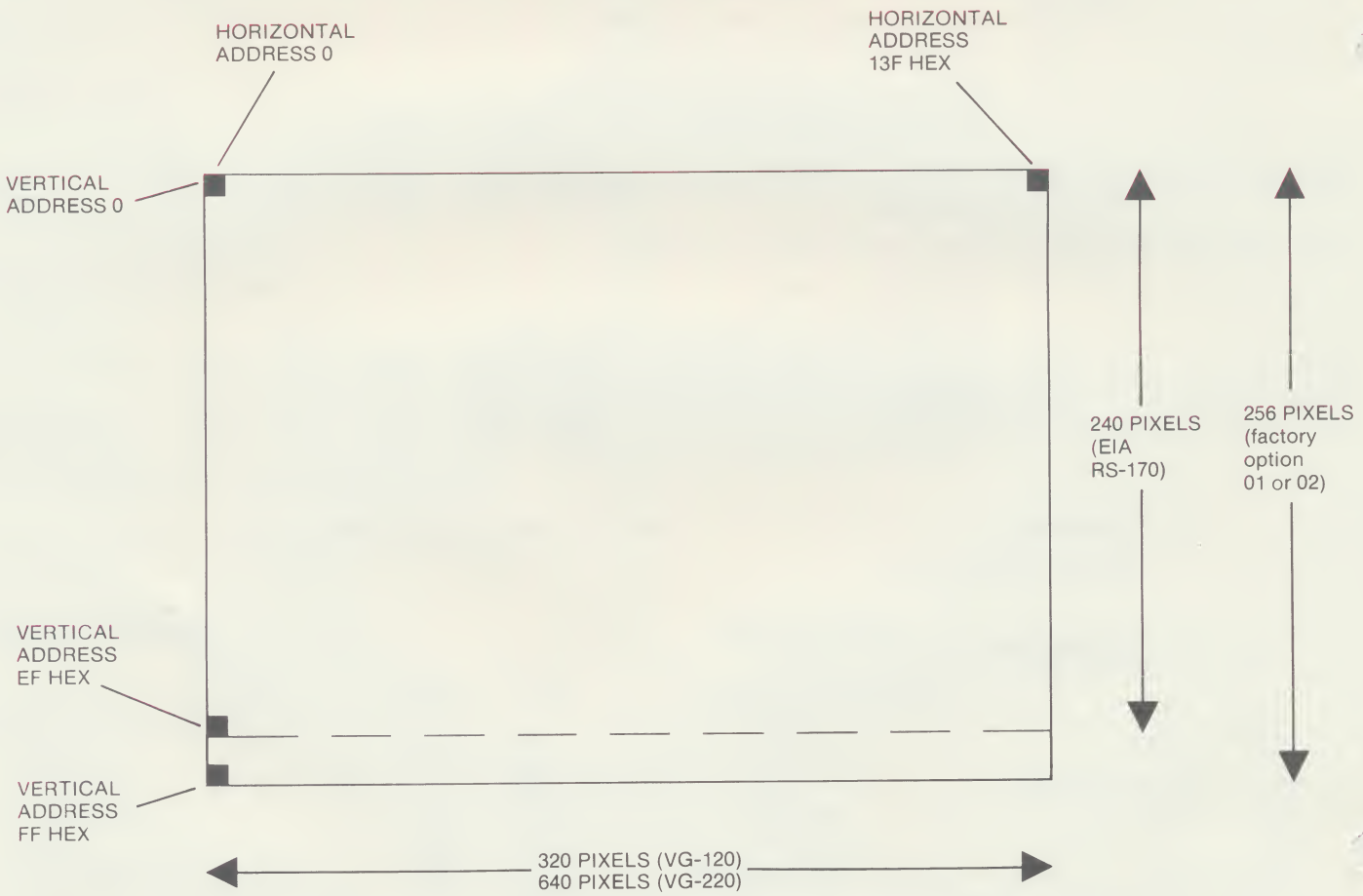
(Assumes screen memory contains valid image.)

1. Initialize registers, as above;
2. Write 01 HEX to Command Port to select post-increment on read;
3. Read Data Port to acquire one pixel of screen data (6-bit models) or two pixels (3-bit models);
4. Write pixel data to desired remote transmission device;
5. Repeat steps 3 and 4 for 81,920 consecutive screen memory locations.

REMOTE RECEPTION

1. Initialize registers and clear screen, as above;
2. Write 02 HEX to Command Port to select post-increment on write;
3. Read pixel data from desired remote reception device;
4. Write pixel data byte to Data Port to store in screen memory (one 6-bit pixel if 6-bit models, two 3-bit pixels if 3-bit models);
5. Repeat steps 3 and 4 for 81,920 consecutive times.

DISPLAY FORMAT

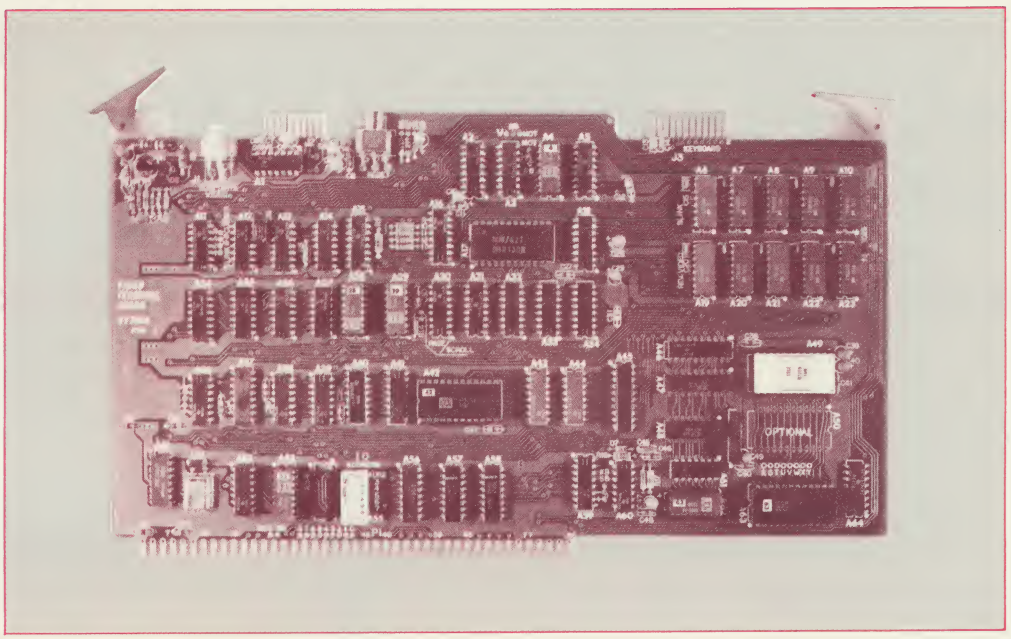


PRINTED IN U.S.A./VG-120/220, R0 8103-10M (DaySys)

DATACUBE INC. ● 670 MAIN STREET ● READING, MA 01867

DATACUBE

VideoTerm
MODELS VT-103 A, B, BP



VideoTerm—your system solution for video display on the Intel MULTIBUS™. Provides I/0 - controlled raster-scan display video for Intel SBC/NSC BLC single-board computers. Allows versatile control of screen, character and cursor displays, using ASCII-type commands. Generates a standard 96-character ASCII font, with any combination of normal, reverse video and blink. Direct cursor positioning is provided to any of the 1024 screen positions, and an on-board keyboard port allows complete video terminal applications.

You choose among models for EIA standard or euro type video generation, at 50 or 60 Hertz. For use where AC mains have erratic frequency, a phase-locked model is offered for a stable display.

- **Intel MULTIBUS™ and NSC Compatible**
- **Full 96-Character ASCII Font**
- **High-Resolution 7x9 Dot Matrix**
- **Any Character Combination of:**
  - **-regular or reverse video**
  - **-blink**
- **High-Density Display — 64 Columns by 16 Lines**
- **Dual Video Outputs**
  - **-direct (X-Y) drive**
  - **-composite video**
- **Direct Cursor Positioning — X-Y (Vector) Address**
- **Program Read of Any Character in Display**
- **Keyboard Input Port — 8 Bits**
  - **-polled or interrupt mode**

Because a full range of byte-oriented commands is provided, your computer program can quickly write (and read) the internal character screen memory. VideoTerm simulates exactly the functions of a standard teleprinter. All operations are through one of four I/O ports provided.

Using standard ASCII commands, simply position the blinking cursor where you want to display a character. Then write the character, using ASCII, or read the one already in screen memory, if desired. For random access to screen memory, position the cursor anywhere by using a 3-byte vector command sequence.

If you require a custom character display font, simply change the on-board plug-in ROM.

Add your composite video or X-Y drive video monitor and a keyboard for a complete video terminal system.

DATACUBE SMK INC. ● 670 MAIN STREET ● READING, MA 01867 ● 617/944-4600

BASIC FEATURES (all models)

COMPATIBILITY: Intel MULTIBUS™(SBC-80 computer series);
National Semiconductor BLC-80 series
CHARACTER FORMAT
CHARACTERS/LINE: 64, fixed
CHARACTER LINES: 16, fixed
FONT: 96 characters, upper/lower case,
mask-ROM generated
MATRIX (HxV): 7x9
BLOCK (HxV): 9x12
CURSOR (addressable): program-selectable for any one screen position
BLINK RATE: 1, 2, 4 or 8 Hz, strap-selected
DISPLAY CHARACTER ATTRIBUTES
REVERSE VIDEO (B-O-W) program-selectable for each
BLINK of 1024 screen positions
BLINK RATE: 1, 2, 4 or 8 Hz, strap-selected
COMPOSITE VIDEO LEVELS: (75-ohm termination)
SYNC 0.0 Volts
BLANK 0.4
BLACK 0.5
WHITE 1.5
DIRECT-DRIVE (X-Y) COMPATIBILITY
Most popular video data displays, including:
BALL BROTHERS, models TV-5, TV-9, TV-12, TV-120
MOTOROLA, models M-1000, M-2000, M-3000, M-4000

MODEL VARIATIONS

MODEL VT-	103A or 103BP	103B or 103BP	103B
VIDEO FORMAT	EIA RS-420	euro	euro
VERTICAL FREQUENCY (Hz)	60.	50.	60.
PERIOD (msec)	16.7	20.	20.
TIMING-HORIZONTAL			
HORIZONTAL FREQ (Khz)	15.72	15.6	15.6
PERIOD (usec)	63.61	64.10	64.10
DLY BEFORE SYNC	1.59	1.60	1.60
SYNC	4.77	4.81	4.81
DLY AFTER SYNC	6.36	6.41	6.41
BLANKING	12.72	12.82	12.82
DRIVE (BALL BROS.)	28.6	28.8	28.8
(MOTOROLA)	4.77	4.81	4.81
TIMING-VERTICAL			
DLY BEFORE SYNC (usec)	190.	192.	192.
SYNC	190.	192.	192.
DLY AFTER SYNC (msec)	1.01	4.23	0.89
BLANKING (msec)	1.34	4.62	1.27
DRIVE (BALL BROS.) (msec)	1.34	4.62	1.27
(MOTOROLA) (usec)	190.	192.	192.

OPTIONS (all models)

ALTERNATE CHARACTER FONTS (special order)	
CABLE ASSEMBLIES (all 3 ft. — 1 M)	PART NO.
KEYBOARD PORT RIBBON CABLE, CONNECTOR	C - 10001
DIRECT-DRIVE RIBBON CABLE, CONNECTOR (for Ball Bros. or Motorola monitor)	C - 10002
COMPOSITE VIDEO CABLE, CONNECTOR	C - 10003
KEYBOARD ASSEMBLY (Models SMK 53, 62, 73 and 86)	
ASCII- encoded, 53 to 86-key, w/cable, connectors	
Solid-state, capacitive-key, N-key rollover	

JUMPER OPTIONS

FUNCTION	PIN-IC POSITION	JUMP PIN FROM	JUMP PIN TO
Vertical Pulse Width (direct drive)	Above A3		
1.34 msec (Ball Bros.)		V	BB
1.90 usec (Motorola)		V	MOT
Horizontal Pulse Width (dir. drive)	Rt of A3		
28.6 usec (Ball Bros.)		H	BB
4.77 usec (Motorola)		H	MOT
Blink Flash Rate (1, 2, 4 or 8 Hz)	Rt of A11	Blink	1,2,4 or 8
Cursor Flash Rate (1, 2, 4, or 8 Hz)	Rt of A11	Cursor	1,2,4 or 8
Page/Scroll	Rt of A29		
Page			— none —
Scroll			— between pins —
Screen Enable	L of A36		
Enable on ASCII NUL, FF and Clear Switch; disable on SOH		(middle pin)	⏚
Disable on ASCII NUL, FF and Clear switch; enable on SOH		(middle pin)	Vcc
Keyboard Strobe Polarity	Rt of A59		
Latch on positive edge		KBSB	+
Latch on negative edge		KBSB	—
Interrupt Request Level	Below		
Keyboard	A53-A55	KB	0 to 7
Ready		RDY	0 to 7
Vertical Frequency (VT103B and BP)	Below A63		
50 Hertz		(middle pin)	50
60 Hertz		(middle pin)	60

DATA AND CONTROL PORTS

WRITE FUNCTION	BIT	READ FUNCTION
KEYBOARD DATA PORT	(base address + 00 HEX)	DISPLAY PORT
Data bit 0	0	Data bit 0 — ASCII control or character byte. Commands range: 00 to 1A HEX; Data range: 20 to 7F HEX
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7 (MSB)	7
	(base address + 01 HEX)	STATUS PORT
	0	Video Status 0=busy; 1=ready
	1	Kybd Data 0=busy; 1=avail
	2	not used
	3	not used
Reserved for future use	4 V0	Cursor vertical position (line number); 0 to F HEX= lines 1 to 16
	5 V1	
	6 V2	
	7 V3	
	(base address + 02 HEX)	CURSOR H PORT
	0 H0	Cursor horizontal position (column position); 00 to 3F HEX=columns 1 to 64
	1 H1	
	2 H2	
	3 H3	
Unused	4 H4	
	5 H5	
	6	Unused
	7	Unused
	(base address + 03 HEX)	CURSOR DATA PORT
	0	Data bit 0 — ASCII character displayed at current cursor position
	1	1
	2	2
	3	3
Unused	4	4
	5	5
	6	6
	7 (MSB)	7

SPECIFICATIONS (all models)

ADDRESSING — I/O

Four I/O ports required, read and write
Strap-selectable to any four-byte boundary
(00, or 04, ... or FC HEX)
No memory address space used

I/O TRANSFER RATE

Read or write (nsec.) : variable, 800 to 1600
Write, incl. scroll (usec): variable 64 to 128
Write, incl. clear screen (msec.) : variable, 8.3 to 16.7

INTERRUPTS

Keyboard interrupt, single-level
Ready interrupt, single-level

Each interrupt is strap-selectable to any one of eight interrupt request levels, and program-enabled

INTERFACES

BUS: All signals TTL-compatible
PARALLEL (keyboard) I/O: All signals TTL-compatible
EXTERNAL SYNC IN (Model VT-103BP only): 6 to 24 Vac, 25 mA; optically-isolated

BUS DESCRIPTION

See Intel Applications Note AP-28

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.5 cm.)
Height: 6.75 in. ref. (17.1 cm.)
Depth: 0.50 in. max. (13. mm.)
Weight: 12 oz. (350 g.)

ELECTRICAL CHARACTERISTICS

DC Power (all voltages ± 5% tolerance):
+5 volts, 2 amperes
+12 volts, 0.1 ampere (VT-103BP — 0.25 ampere)
-12 volts, 0.1 ampere (VT-103BP — 0.15 ampere)

ENVIRONMENTAL

Temperature:
Operating: 0 to 55°C (32 to 131°F)
Storage: -40 to 100°C (-40 to 212°F)

CONNECTORS

INTERFACE	NO. OF PINS	CENTERS (IN)	MATING CONNECTORS
Bus	86	0.156	CDC VPB01E43A00A1
Keyboard	26	0.100	3M 3462-0001 or TI H312113
VIDEO			
Direct Drive	20	0.100	3M 3461-0001
Composite	2	0.156	MOLEX 09-50-3021

PROGRAMMING NOTES

BASIC READ OR WRITE SUBROUTINE

1. Test VideoTerm for Ready status, signifying its availability for I/O read or write operations. Test can be by polling Status Port or by interrupt request, if enabled; when status is Ready:

2a. Write data in computer register "A" to VideoTerm by executing an OUT instruction to the Display Port; or:

2b. Read data to computer register "A" from VideoTerm by executing an IN instruction from the Cursor Data Port;

3. Exit subroutine.

INITIALIZE ROUTINE

1. Power-up is equivalent to ASCII FF (0C HEX) written to Display Port to:
   - clear entire screen;
   - return cursor to home position;
   - clear all attribute and interrupt enables and attribute flags;
   - enable screen display (jumper option);
2. Write ASCII SOH (01 HEX) to Display Port to enable screen display — only if jumper option disabling screen on ASCII FF is used;
3. Enable desired attributes for entire screen by writing control characters to Display Port:
   - write ASCII ETX (03 HEX) to enable reverse video;
   - write ASCII DC1 (11 HEX) to enable blink;
4. Enable desired interrupts by writing control characters to Display Port:
   - write ASCII CAN (18 HEX) to enable Ready interrupt;
   - write ASCII SUB (1A HEX) to enable keyboard interrupt.

CHARACTER DISPLAY ROUTINE

1. Enable desired attribute flags for character to be displayed by writing control characters to Display Port:
   - write ASCII ENQ (05 HEX) to set reverse video attribute;
   - write ASCII DC2 (12 HEX) to set blink attribute;

2a. Move cursor to desired screen position by writing control character to Display Port (see Cursor Controls); or:

2b. Use direct cursor address sequence to move cursor to any desired screen location (see Direct Cursor Positioning Controls);

3. Fetch character (range 20 to 7F HEX) to be written at current cursor position and write it to Display Port — cursor will increment to next position;
4. Go to step 2 or 3 as required by location of next character.

DISPLAY MEMORY READ

1. Position cursor to desired character position as in CHARACTER DISPLAY ROUTINE, step 2a or 2b;
2. Read and store character data available at Cursor Data Port — cursor does not increment to next character;
3. Go to step 1 for next character.

CONTROL COMMANDS

Write these commands to Display Port to control VideoTerm functions.

Screen Controls* — Control video output from display memory

ASCII NUL (00 HEX): Enable Screen Display — unblanks display

ASCII SOH (01 HEX): Disable Screen Display — blanks display

ASCII FF (0C HEX): Clear Screen Display — clears display, returns cursor to home position, resets all flags and enables

Screen Attribute Controls — control display of attributes for entire screen

ASCII STX (02 HEX): Disable Reverse Video — all characters displayed regular video (W-O-B)

ASCII ETX (03 HEX): Enable Reverse Video — characters with reverse video flag set displayed reverse video (B-O-W)

ASCII DLE (10 HEX): Disable Blink — all characters displayed without blink

ASCII DC1 (11 HEX)*: Enable Blink — characters with blink flag set are displayed as blinking

Character Attribute Latch Controls — When attribute is enabled, each character entered thereafter is flagged in display memory for that attribute; when attribute is disabled, character not flagged.

ASCII EOT (04 Hex): Reverse Video Flag Off

ASCII ENQ (05 HEX): Reverse Video Flag On

ASCII DC2 (12 HEX): Blink Flag On

ASCII DC4 (14 HEX): Blink Flag Off

Cursor Controls — move cursor to defined position within display memory; no change in displayed character

ASCII BS (08 HEX): Backspace— moves cursor one position left; no effect if cursor already at column one

ASCII HT (09 HEX): Space — moves cursor one position right; if cursor at last column, moves cursor to first column of next lower line

ASCII LF (0A HEX): Line Feed — moves cursor down one line in same column

ASCII VT (0B HEX): Reverse Line Feed — moves cursor up one line in same column; no effect if cursor on first line

ASCII CR (0D HEX): Carriage Return — moves cursor to column one of current line

ASCII SO (0E HEX): Home — moves cursor to line one, column one

ASCII DC3 (13 HEX): New Line — combined Carriage Return and Line Feed cursor functions

Direct Cursor Positioning — moves cursor directly to any screen position, using a three-command sequence

1. ASCII SI (0F HEX): begin position sequence
2. XXXX NNNN BINARY, where NNNN (0 to F HEX) defines cursor position on one of lines 1 to 16
3. XXNN NNNN BINARY, where NN NNNN (00 to 3F HEX) defines a cursor position in one of columns 1 to 64

Interrupt Controls* — control interrupt enables

ASCII ETB (17 HEX): Disable Ready Interrupt — inhibits interrupt on Ready status

ASCII CAN (18 HEX): Enable Ready Interrupt — enable interrupt on Ready status (when VideoTerm is ready for I/O read or write)

ASCII EM (19 HEX): Disable Keyboard Interrupt — inhibits interrupt on Keyboard Data Ready

ASCII SUB (1A HEX): Enable Keyboard Interrupt — enables interrupt on Keyboard Data Ready (when valid data is present in keyboard latch)

* Control functions shown with asterisk are affected by jumper options. See jumper table for details.

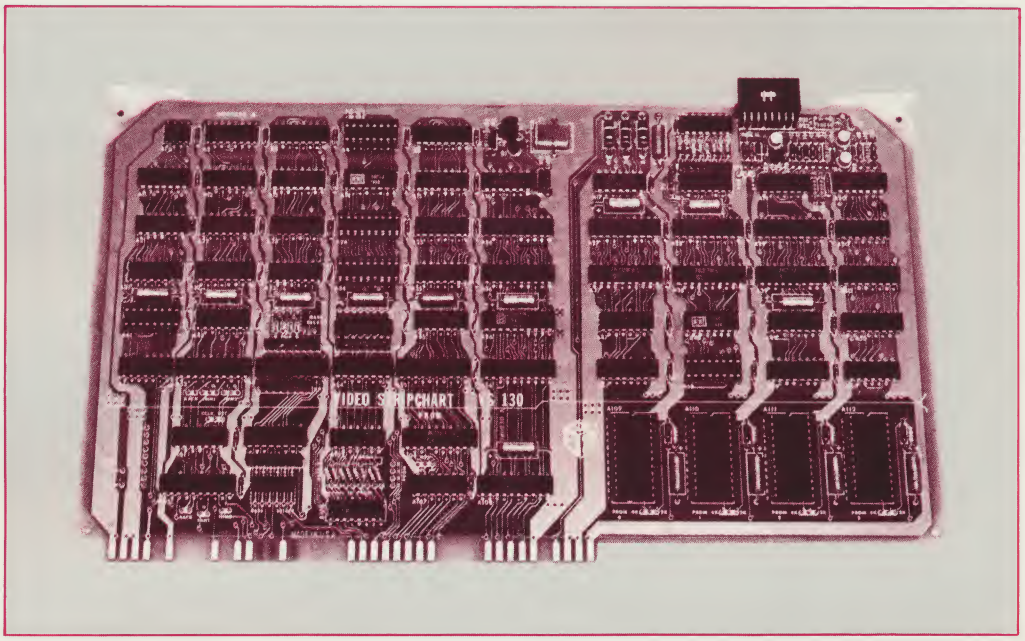
X in BINARY bit sequence indicates that bit is unused, and may be either 0 or 1.

PRINTED IN U.S.A. / VT-103, RO 7805-1M (DAY)

DATACUBE SMK INC. ● 670 MAIN STREET ● READING, MA 01867

Datacube INC.

VIDEO STRIP CHART
MODEL VS-130



Video display generation of four independent events, simulating the format of a strip-chart recorder, but using no paper. Simultaneous display of one to four pseudo-analog channels, as well as a superimposed graticle, in either B&W or color.

A bonus of 16 kilobytes of ROM/PROM sockets for MULTIBUS memory expansion.

- **Intel MULTIBUS™ & NSC Compatible**
- **Four Independent Event Channels**
- **Pseudo-Analog Display with Eight-Bit Resolution (1/256)**
- **Black & White or R-G-B Color Display**
- **EIA-Standard RS-420 Video Output**
- **Full Computer Access to Screen Memory — Horizontal and Vertical for Graticle**
- **Automatic Scroll from Top or Bottom**
- **Selectable Display Format for:**
  - **— Line Width**
  - **— Graticle**
  - **— Channel Selection**
  - **— Illuminance or Color**
- **Independent Memory Section:**
  - **— Accepts max 16 KB ROM or PROM Devices**
  - **— Full 20-Bit MULTIBUS Address Decode; Select Address on any 16K Boundary**
  - **— Accepts Industry-Standard PROM or ROM Devices**
  - **— Sockets for Four 2716 or 2732-Type Devices**
  - **— Selectable Access Time and Device Active**

Your MULTIBUS-based computer provides 8-bit data values to VS-130, which are stored in on-board memory and displayed on a standard video monitor in strip-chart format.

Under program control, VG-130 can display one to four independent strip chart channels on an EIA-standard video monitor in either black-and-white or R-G-B color. Choose automatic scroll from either top or bottom of the display to simulate a window to a moving strip chart. Add horizontal or vertical lines to create a display graticle for accurate reading.

Select unique colors (or illuminance) for each channel and also for horizontal and vertical grids.

You can perform direct read/write operations on any display data, to analyze channel information, or to perform display enhancements.

The on-board PROM/ROM memory adds a bonus of MULTIBUS memory, totally independent from other VS-130 functions.

DATACUBE INC. • 670 MAIN STREET • READING, MA 01867 • 617/944-4600 TWX 710/393-0144

SPECIFICATIONS

MEMORY ADDRESSING

General

VS-130 addressing is controlled by two separate sections, one for Display Memory, the other for ROM/PROM memory. ROM/PROM memory addressing and bus response are totally independent of display memory.

MULTIBUS signals INH1 and INH2 are both implemented, and may be either inputs or outputs. They provide overlay control for RAM and ROM according to MULTIBUS specifications.

Display Memory

On-board display read-write memory, 256 x 8 bits — memory-mapped. The first 240 locations are display memory and the last 16 are for control. See Address Map below.

Full 20-bit MULTIBUS address decode; DIP switch select display memory base address to appear on any 256-byte boundary anywhere within the 1-megabyte range. (VS-130 is shipped with base address 5000 HEX selected.)

ROM/PROM Memory

Sockets for maximum 16 kilobytes industry-standard ROM, PROM or EPROM. Accepts any combination of one to four 2716 or 2732 5-volt EPROM devices, or pin-compatible ROM or PROM. Sockets are addressed as sequential, non-overlapping memory.

Full 20-bit MULTIBUS address decode; strap-select ROM/PROM memory base address to appear on any 16K boundary anywhere within the 1-megabyte range.

Access time strap-selectable for devices in the range 50 to 1500 nsec. All installed devices must have access times equal to or faster than that selected.

Independent strap-select activity for each socket; devices which are in inactive sockets provide no bus acknowledge.

INTERFACES

Bus: All signals TTL-compatible

Composite Video: 75-ohm output, composite sync provided on the green/B&W video channel.
- 60 Hz — EIA standard RS-420 compatible (525 lines, non-interlaced)
- 50 Hz — 625 lines, non-interlaced)

Video Sync: TTL-compatible output.

BUS DESCRIPTION

See Intel MULTIBUS Applications Note AP-28A and IEEE 796 proposed bus standard.

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.5 cm.)
Height: 6.75 in. ref. (17.1 cm.)
Depth: 0.5 in. max. (13 mm.)
Weight 20 oz. (570 g.) approx.

ELECTRICAL CHARACTERISTICS

DC Power (all voltages ± 5% tolerance):
- +5 volts, 3 amperes
- +12 volts. 0.05 ampere
- −12 volts, 0.05 ampere

ENVIRONMENTAL

Temperature:
- Operating: 0° to 55°C (32° to 131°F)
- Storage: -40° to 100°C (-40° to 212°F)

Humidity: 10 to 90% RH, non-condensing

CONNECTORS

INTERFACE	NO. OF PINS	CENTERS (in.)	MATING CONNECTORS
BUS	86	0.156	CDC VPB01E43A00A1
VIDEO Output Pin (F)	16	0.100	AMP 1-87631-2 AMP 87045-2

VIDEO CONNECTOR ASSIGNMENTS

Connector J1, Video Output:

PIN	DESCRIPTION	PIN	DESCRIPTION
	composite video:		
1	Green or B&W	2	ground, video
3	Blue	4	ground, video
5	Red	6	ground, video
7	n/c	8	ground, digital
9	n/c	10	ground, digital
11	n/c	12	ground, digital
13	composite sync	14	ground, digital
15	n/c	16	ground, digital

n/c: no connection

VIDEO TIMING

HORIZONTAL TIMING

Horizontal Freq. (KHz)	15.72
Timing in microseconds:	
Period	63.6
Active Scan	46.7
Front Porch	1.59
Sync	4.77
Back Porch	6.36
Blanking	12.7

VERTICAL TIMING

VERTICAL FREQUENCY (Hz)	60	50
Timing in milliseconds:		
Period	16.7	20.0
Active	15.2	16.4
Equalizing	0.190	0.190
Sync	0.190	0.190
Blanking	1.43	1.43
Dot Clock (MHz)	5.48	5.48
CPS Access Time (nsec, avg.)	814.	800.

ADDRESS MAP (video section only)

BASE means a base address, which is strap-selectable to any 256-byte boundary within the MULTIBUS address range.

ADDRESS	ASSIGNMENT	DESCRIPTION
		Read/Write:
BASE + 0 to BASE + EF HEX	Display Bottom to Display Top	Screen-mapped video RAM, 240 bytes
		Write-Only:
BASE+F0 HEX	CHAN 0 BOTTOM	Bottom entry, scrolls up
BASE+F1 HEX	CHAN 1 BOTTOM	Bottom entry, scrolls up
BASE+F2 HEX	CHAN 2 BOTTOM	Bottom entry, scrolls up
BASE+F3 HEX	CHAN 3 BOTTOM	Bottom entry, scrolls up
BASE+F4 HEX	HORIZ GRID BOTTOM	Bottom entry, scrolls
BASE+F5 HEX	VERT GRID ON	Vertical Grid on at line 00 to EF HEX
BASE+F6 HEX	VERT GRID OFF	Vertical Grid off at line 00 to EF HEX
BASE+F7 HEX	— not assigned —	
BASE+F8 HEX	CHAN 0 TOP	Top entry, scrolls down
BASE+F9 HEX	CHAN 1 TOP	Top entry, scrolls down
BASE+FA HEX	CHAN 2 TOP	Top entry, scrolls down
BASE+FB HEX	CHAN 3 TOP	Top entry, scrolls down
BASE+FC HEX	HORIZ GRID TOP	Top entry, scrolls down
BASE+FD HEX	— not assigned —	
BASE+FE HEX	VIDEO ENABLE	Enable video output
BASE+FF HEX	COMMAND PORT	Select channel access, scroll

DATA AND CONTROL PORTS (memory addresses)

BASE +	PORT	FUNCTION
F0 HEX	CHAN. 0 BOTTOM	write horiz. position as byte 00 to FF HEX; enters data to display memory at current line. If this is the selected scroll control channel, scrolls all channels from bottom to top by one line and displays next line of each active channel.
F1 HEX	CHAN. 1 BOTTOM	same as CHAN. 0 BOTTOM, except for Chan. 1
F2 HEX	CHAN. 2 BOTTOM	same as CHAN. 0 BOTTOM, except for Chan. 2
F3 HEX	CHAN. 3 BOTTOM	same as CHAN. 0 BOTTOM, except for Chan. 3
F4 HEX	HOR. GRID BOTTOM	7 6 5 4 3 2 1 0 not used 0 blank line 1 horizontal line same as CHAN. 0 BOTTOM, except for a horizontal line or blank, according to Bit 0
F5 HEX	VERT. GRID ON	write position of vertical line as data byte 00 to FF HEX (direct select — no scroll)
F6 HEX	VERT. GRID OFF	same as VERT. GRID ON, except blank line
F7 HEX	— not assigned —	
F8 HEX	CHAN. 0 TOP	write horiz. position as byte 00 to FF HEX; enters data to display memory at current line. If this is the selected scroll control channel, scrolls all channels from top to bottom by one line and displays next line of each active channel.
F9 HEX	CHAN. 1 TOP	same as CHAN. 0 TOP, except for Chan. 1
FA HEX	CHAN. 2 TOP	same as CHAN. 0 TOP, except for Chan. 2
FB HEX	CHAN. 3 TOP	same as CHAN. 0 TOP, except for Chan. 3
FC HEX	HORIZ. GRID TOP	(same as CHAN. 0 TOP, except scrolls from top to bottom)
FD HEX	— not assigned —	
FE HEX	VIDEO ENABLE	7 6 5 4 3 2 1 0 not used channel 0 enable channel 1 enable channel 2 enable channel 3 enable vertical enable horizontal enable 0=enable, 1=disable NOTE: for wide channels, enable BOTH narrow channels implied.
FF HEX	COMMAND PORT	7 6 5 4 3 2 1 0 not used 000 scroll on write to chan 0 001 scroll on write to chan 1 010 scroll on write to chan 2 011 scroll on write to chan 3 100 scroll on write to horiz. 1x1 — not used — 0 disable scroll 1 enable scroll 00 select channel 0 mem bank 01 select channel 1 mem bank 10 select channel 2 mem bank 11 select channel 3 mem bank

PROGRAMMING NOTES

Refer to the Data and Control Ports and Display Format for this discussion.

A strip chart format represents a stream of continuously-updated data which scrolls from an origin. VS-130's display represents a fixed window to such a stream, where the data may scroll from either the top or bottom of the display. As the data enter, they are entered sequentially into display RAM. (Data which scroll past the window are old, or overflow, and are lost.)

Each data byte stored in display memory represents one of 256 horizontal positions (columns) for the display marker representing one channel, where a zero value is the left side, and FF HEX is the right side. The marker's vertical position, or "chart track," is determined by the sequential values written into the 240 display locations.

Data bytes may be read or written to display RAM in the same manner as any memory on the MULTIBUS. However, strip chart format implies sequential entry from top or bottom, with automatic scroll of the display. By writing a byte to a data port, you both store the value in display memory as a horizontal position for one channel, and automatically increment an internal pointer, which advances that channel to the next vertical position (line). The same function occurs for horizontal lines. The pointer may advance either from bottom to top or top to bottom of display memory, according to the chosen data port.

The Command Port permits you to select one channel (or the horizontal grid) to control display scroll. When that channel's port is written to, the entire display scrolls to the current vertical position, displaying all channels. Data in display memory for other channels is not displayed until this event.

Access to display RAM on the MULTIBUS is by bank, one for each of the four channels. The Command Port selects which one of the memory banks appears on the bus.

A Video Enable Port controls which of the four channels and the horizontal and vertical grids are allowed to be displayed.

Vertical grids are added or deleted individually to one of 256 display memory locations, by writing to either of the two vertical control ports. Display scroll has no effect on these grids, except to advance them along with data from each channel.

OUTPUT FORMAT SELECTION

VS-130 provides eight simultaneous output display sources, shown in the table below. Each source to be included in the video display must be strapped to a display control output which determines the color (or illuminance level, if B&W) of that source. (If no strap is made, the display will be blank.)

All sources are open-collector, and can be wire-or'ed in any combination. This means that different sources may be the same color; simply connect them to the same control output.

Wide line channels are formed internally by combining sources from two channels to form a wide line on the display. For example, Channel W12 combines Channels 1 and 2 to form a wide video line. This line starts at the Channel 1 value (position) and ends at the Channel 2 value. In the same way, Channel W34 is formed from Channels 3 and 4. (For correct operation, the minimum end-point value of a wide channel must be its starting value plus one.)

FORMAT CONTROL TABLE

VIDEO SOURCE		OUTPUT CONTROL		
	PIN	B&W	COLOR	PIN
CHANNEL 1	N0	BLACK	BLACK	OUT0
CHANNEL 2	N1	GRAY 1	RED	OUT1
CHANNEL 3	N2	GRAY 2	BLUE	OUT3
CHANNEL 4	N3	GRAY 3	VIOLET	OUT4
CHANNEL W12	W12	GRAY 4	GREEN	OUT5
CHANNEL W34	W34	GRAY 5	YELLOW	OUT6
VERT GRID	V	GRAY 6	CYAN	OUT7
HORIZ GRID	H	WHITE	WHITE	OUT8

OPTION STRAP SUMMARY

Display Memory Base Address
Described in the Memory Addressing section. Straps or switches located above A53 and A54. MULTIBUS address bits labeled from 0H HEX to 13 HEX, and are logic 1 when connected, or the switch is in the ON or 1 position.

ROM/PROM Memory Base Address
Described in the Memory Addressing section. Straps located above A106, and labeled as address bits 0E HEX to 13 HEX. Program in the same way as Display Memory base address.

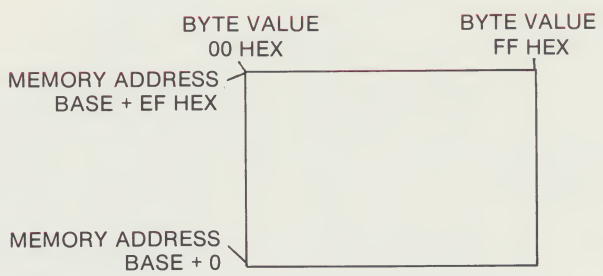
Inhibit Bus Signals — INH1 and INH2
Described in the Memory Addressing section.

Advanced Acknowledge Bus Signal
Install AACK EN jumper to enable Advanced Acknowledge. This signal has the same timing as Transfer Acknowledge (XACK/), and does not provide advanced timing. AACK is no longer a supported MULTIBUS signal.

Vertical Frequency
Jumper to select either 50 or 60 Hz vertical frequency. Three pins, located above A4; strap the center pin to either the "50" or "60" pin.

Output Format
Described in the Output Format Selection section. Pins are located below A8.

DISPLAY FORMAT



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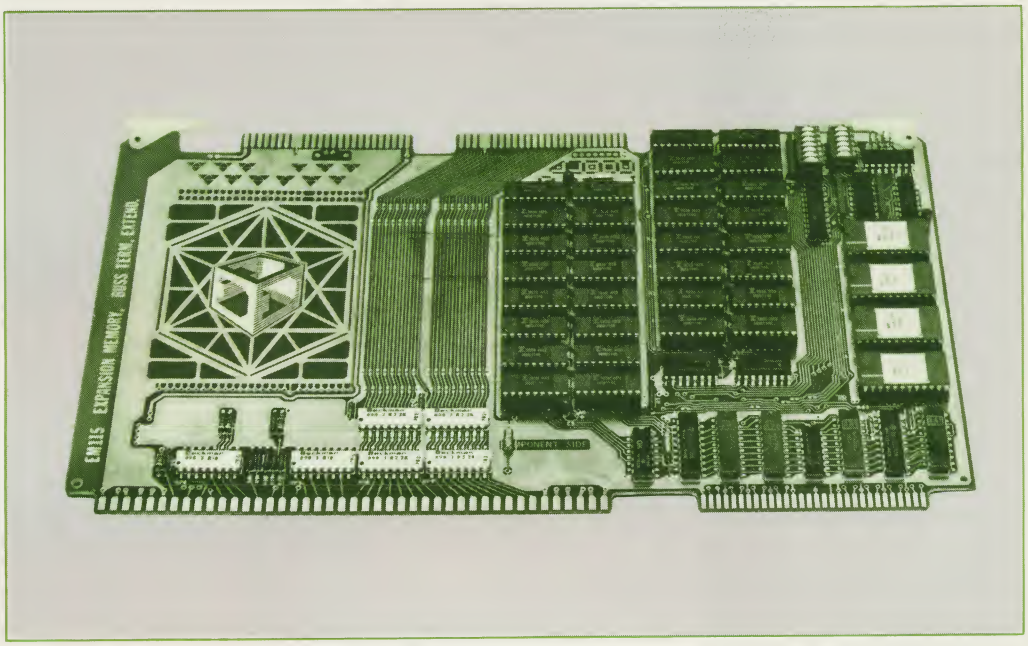
Datacube INC.

MODEL EM-115
DUAL-PORT MEMORY EXPANSION



Efficient interconnection module for the RM-117 dual-port memory management system. Extends the RM-117's Port B to a second MULTIBUS™-compatible card cage. Provides termination of all bus lines. A version available with expansion RAM and ROM memory, for access by RM-117.

- **Intel MULTIBUS™ and NSC Compatible**
- **PROM/ROM Feature Provides Four 2KB PROM/ROM Sockets — Each Socket Independently Enabled**
- **20-Bit Address Bus—Also Compatible with 16 Bits**
- **Full MULTIBUS™ Termination**
- **All Required Interconnection Cables Provided**
- **Two Versions:**
  - **—Dual-Port MULTIBUS™ Connector/Terminator (for RM-117)**
  - **—As Above, with 16KB RAM and Sockets for 8KB PROM or ROM**
- **Read/Write Memory Option: Low-Power 2114-Type Static Memory for RM-117 Access**

For true multiprocessor performance on the MULTIBUS™, use EM-115 paired with RM-117. An RM-117 gives you dual-port memory with full-featured management. EM-115 connects an RM-117 to your second MULTIBUS™ system.

Because each of your processors has full and independent control over its own bus, no contention delays can occur to degrade performance. Yet, each system can flexibly access as much as one megabyte of common memory controlled by RM-117. Because EM-115 provides full bus termination, no backplane-mounted resistors are required.

EM-115 is available with an optional 16 kilobytes of RAM and sockets for 8 kilobytes of ROM or PROM, to allow more complete use of module space.

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SPECIFICATIONS

BUS COMPATIBILITY

Module (P1) connector: full MULTIBUS™ compatibility; extends RM-117 B port to a second MULTIBUS™. Provides resistive termination for MULTIBUS™ signals.

Module (P2) connector: provides memory bank select signals for DATACUBE-compatible modules.

Top-edge connectors (2): interconnection for RM-117 PORT B; also compatible with Intel MDS Series II development system external expansion bus.

MEMORY ADDRESSING

Memory is optional; if provided, it is addressed as expansion for the RM-117. Twenty-bit address selection is provided. Internal pull-up resistors default the 4 MSB address bits to zero, to make the EM-115 compatible with a 16-bit address system.

Read/write memory: one bank of 16 kilobytes static RAM. The 200-nsec. access time allows maximum RM-117 speed. Address origin selected by DIP slide switches to any 16K boundary.

Read-only memory: accepts one to four industry-standard 24-pin 5-volt, 2K x 8 ROM or bipolar PROM devices (e.g.: 82S191/3636 PROM, 6276 ROM). Maximum permissable access time for any device is 200 nsec. Individual jumper enable for each device. Address origin selected by DIP slide switches to any 8K boundary.

DATA BUS

Eight-bit data, MULTIBUS™-Compatible

BUS DESCRIPTION

All signals TTL-compatible

See Intel Applications Note AP-28A.

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.5 cm.)
Height: 6.75 in. ref. (17.1 cm.)
Depth: 0.50 in. max. (13 mm.)
less user-installed PROMs
Weight: 12 oz. (340 g.), fully-populated

ELECTRICAL CHARACTERISTICS

DC Power (voltage ±5% tolerance):
+5 volts, 0.1 ampere, unpopulated
2.5 amperes max., fully-populated
(also add current of user-installed PROMs.)

ENVIRONMENTAL

Temperature:
Operating: 0 to 55° C (32 to 131° F)
Storage: -40 to 100° C (-40 to 212° F)
Humidity: 10 to 90% RH, non-condensing

CONNECTORS

INTERFACE	NO. OF CONTACTS	CENTERS (in.)	MATING CONNECTORS
RM-117 Port B	2 x 50	0.100	3M 3415-0001
MULTIBUS™			
P1	86	0.156	CDC VPB01E43A00A1
P2	60	0.100	CDC VPB01B30A00A1

VERSIONS

EM-115-UP MULTIBUS™ extender for RM-117 Port B, including resistive bus terminators
EM-115-016 As above, also including installed 16 kilobyte static RAM and 8 kilobyte PROM/ROM capability (4 x 2 KB)

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